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LKS32MC03x with built-in 3P3N Gate Driver

32bit Compact MCU for Motor Control

Features

- 48MHz 32-bit Cortex-M0 core, hardware division coprocessor
- low-power sleep mode, MCU sleep power consumption is 30uA
- -40-105℃ industrial-grade operating temperature range
- Super antistatic and anti-group pulse capability

Storage

- 32kB flash, with a flash anti-stealing feature
- 4kB RAM

Timer

- Built-in 4MHz high-precision RC timer, with a full temperature range accuracy of ±1%
- Built-in 64kHz low-speed timer for use in low-power mode
- Internal PLL providing up to a 48MHz timer

Peripherals

- One UART
- One SPI
- One IIC
- General-purpose 16-/32-bit timer, supporting capture and edge-aligned PWM
- Dedicated PWM module for motor control, supporting 6 PWM outputs, independent dead zone control
- Dedicated interface for Hall signals, supporting speed measurement and debounce
- 4-channel DMA
- Hardware watchdog
- Supports up to 25 GPIOs

Analog Module

- Integrated one 12-bit SAR ADC, 1.33Msps sampling and conversion rate, 14 channels in total
- Integrated 2 OPA, settable for a differential PGA mode
- Integrated two comparators
- Integrated 8-bit DAC digital-to-analog converter as an internal comparator input
- Built-in 1.2V voltage reference with an accuracy of 0.5%
- Built-in 1 low-power LDO and power monitoring circuit
- Integrated high-precision, low-temperature drift high-frequency RC timer

Key Strengths

✧ The internal integration of 2 high-speed operational amplifiers can meet the different requirements of single-resistor/dual-resistance current sampling topology;

✧ The input port of the operational amplifier integrates a voltage clamp protection circuit, and only two external current-limiting resistors are needed to achieve direct current sampling of the MOSFET internal resistance;

✧ ADC module variable gain technology can work with high-speed operational amplifiers to handle a wider dynamic range of current and take into account the sampling accuracy of small current and large current;

✧ Integrated two-way comparator;

✧ Strong ESD and anti-interference ability, stable and reliable;

✧ supply to ensure the versatility of system power supply.

✧ Supports IEC/UL60730 functional safety certification

Application Scenarios

Applicable to control systems such as BLDC/ Sensorless BLDC/ FOC/Sensorless FOC and stepping motors, permanent magnet synchronous motors, asynchronous motors, digital power source etc.

1 Overview

1.1 Function Description

The LKS32MC03x_3P3N series are 32-bit core compact MCU intended for motor control applications that integrates all the modules required for common motor control systems. tha t integrate three pairs of P-N MOSFET driver modules and can drive 3 pairs of P-N MOSFET s directly. Some models have integrated PN-MOS.

- **Performance**
  - 48MHz 32-bit Cortex-M0 core
  - Low-power sleep mode
  - Integrated three-phase full-bridge bootstrapping gate drive modules
  - Industrial-grade operating temperature range
  - Super antistatic and anti-group pulse capability

- **Memory**
  - 32 kB Flash with encryption, a 128-bit chip unique identifier
  - 4kB RAM
- **Operating Range**
  - Operating temperature: -40~105℃
- **Timer**
  - Built-in 4MHz high-precision RC timer, with an accuracy within ±1% in a range of -40~105℃
  - Built-in 64kHz low-speed timer for use in low-power mode
  - Internal PLL providing up to a 48MHz timer
- **Peripheral Module**
  - One UART
  - One SPI for master-slave mode
  - One IIC for master-slave mode
  - One general-purpose 16-bit timer, supporting capture and edge-aligned PWM functions
  - One general-purpose 32-bit timer, supporting capture and edge-aligned PWM functions;
  - Dedicated PWM module for motor control, supporting 8 PWM outputs, independent dead zone control
  - Dedicated interface for Hall signals, supporting speed measurement and debounce functions
  - Hardware watchdog

- 25 GPIOs. Eight GPIOs can be used as wake-up sources for the system. 17 GPIOs can be used as external interrupt source inputs

- **Analog Module**
  - Integrated one 12-bit SAR ADC, 1.33Msps sampling and conversion rate, 14 channels in total
  - Integrated a 2-channel operational amplifier, settable for a differential PGA mode
  - Integrated two comparators
  - Integrated 8-bit DAC digital-to-analog converter
  - Built-in ±2°C temperature sensor
  - Built-in 1.2V voltage reference with an accuracy of 0.5%
  - Built-in 1 low-power LDO and power monitoring circuit
  - Integrated high-precision, low-temperature drift high-frequency RC timer

- **Packaging:**

Table 1-1 Summary of LKS32MC03x Package Models

Model	Package Type
LKS32MC031KLC6T8	LQFP48
LKS32MC033H6P8	TSSOP20
LKS32MC033H6Q8	QFN20
LKS32MC034DF6Q8	QFN40
LKS32MC034DOF6Q8	QFN40
LKS32MC035DL6S8	SOP16
LKS32MC035EL6S8	ESOP16
LKS32MC037M6S8	SSOP24
LKS32MC037EM6S8	SSOP24
LKS32MC037FM6S8	SSOP24
LKS32MC037QM6Q8	QFN24
LKS32MC038Y6P8	TSSOP28
LKS32MC039DK6Q8B	QFN32
LKS32MC039PL5K6Q8B	QFN32
LKS32MC039PL3K6Q8B	QFN32

1.2 Key Strengths

- High reliability, high integration, small volume of final product, saving BOM costs.
- Internally integrated 2-channel high-speed operational amplifier and two comparators to meet the different requirements of single-resistor/dual-resistor current sampling topologies;
- Internal high-speed operational amplifier integrating high-voltage protection circuits, allowing the high-level common-mode signal to be directly input into the chip, and realizing the direct current sampling mode of MOSFET resistance with the simplest circuit topology;
- The application of patented technology enables the ADC and high-speed operational ampli-

fier to match best, which can handle a wider current dynamic range, while taking into account the sampling accuracy of high-speed small current and low-speed large current;

- The overall control circuit is simple and efficient, with stronger anti-interference ability, more stable and reliable;
- Integrated three-phase full-bridge bootstrapping gate drive modules; LKS32MC039PL5K6Q8B/ LKS32MC039PL3K6Q8B integrates a three-phase full bridge circuit composed of three pairs of MOS;

Applicable to control systems such as inductive BLDC/non-inductive BLDC/inductive FOC/non-inductive FOC and stepping motors, permanent magnet synchronous motors, asynchronous motors, etc.;

1.3 Naming Conventions

LKS32 MC 037 D 2 M 6 S 8 B (XX)

Device series

LKS32	= 32bit MCU
LKS5	= Gate Driver Products
LKS6	= Power IC Product

Product type

MC	= Motor Control Applications
AT	= Automobile Applications
RV	= RISC-V for Motor Control

Device sub family

031KL	= 1 ADC, 2 PGA, 6N Driver, 5V LDO
033	= 1 ADC, 2 PGA
034D	= 1 ADC, 2 PGA, 6N Driver
034DO,034F,032F	= 1 ADC, 2 PGA, 6N Driver, 5V LDO
034S	= 1 ADC, 2 PGA, 6N Driver, 5V LDO, DBOOT
035D,035E,039E	= 1 ADC, 1 PGA, 3P3N Driver, 5V LDO
033,037,038	= 1 ADC, 2 PGA
037E,037F,039,031	= 1 ADC, 2 PGA, 3P3N Driver, 5V LDO
037L,038L,038Y	= 1 ADC, 2 PGA, 5V LDO
039PL5	= 1 ADC, 2 PGA, MOS, 5V LDO
039PL3	= 1 ADC, 2 PGA, MOS, 3.3V LDO

Gate Driver Functions

D	= 3P3N Gate Driver
E/DL	= 3P3N + 5V LDO
S/F	= 6N Gate Driver
SL/FL	= 6N + 5V LDO
K	= High V 6N Gate Driver
O/L5	= 5V LDO/DCDC
L3	= 3.3V/3V LDO
N	= DCDC
P	= 3P3N/4P4N DrMOS
Q	= 6N/8N DrMOS
PL3	= 3P3N DrMOS + 3.3VLDO
PL5	= 3P3N DrMOS + 5VLDO
QL	= 6N DrMOS + LDO
X	= PHY
XL	= PHY + LDO

PKG/Driver Ver

2	= 2nd Ver
S	= S 侧面上锡

Pin count

L	=16 pins
H	= 20 pins
M	= 24 pins
Y	=28 pins
K	= 32 pins
F	= 40 pins
G	= 42 pins
U	= 44 pins
C	= 48 pins
N	= 52 pins
S	= 54pins
E	= 60 pins
R	= 64 pins
P	= 80 pins
V	=100 pins
Q	=128 pins
Z	=144 pins

Code size

4	= 16Kbyte Flash Memory
6	= 32Kbyte Flash Memory
8	= 64Kbyte Flash Memory
B	=128Kbyte Flash Memory
C	=256Kbyte Flash Memory
D	=384Kbyte Flash Memory
E	=512Kbyte Flash Memory

Package

P	= TSSOP
T	= TQFP/LQFP
Q	= QFN
S	= SSOP
H	= BGA

Temperature range

6	= -40~85°
8	= -40~105°
9	= -40~125°

MCU Ver

B	= B ver

Options

TR	= Tape and reel packing
P	= ES

Figure 1-1 LKS32MC03x Device Naming Conventions

2 Device Selection Table

Table 2-1 LKS03x Series Device Selection Table

	Frequency (MHz)	Flash (kB)	RAM (kB)	ADC ch.	DAC	Comparator	Comparator ch.	OPA	HALL	SPI	IIC	UART	Temp. Sensor	PLL	Gate driver	Gate Driver current (A)	Pre-drive supply (V)	Gate floating voltage (V)	Others	Package
LKS32MC031PC6Q8C*	48	32	4	9	8BITx1	2	6	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	5.7-28		5V LDO	DFN5.0*6.0 48L
LKS32MC033PH6Q8C	48	32	4	7	8BITx1	2	5	1	3	1	1	1	Yes	Yes						QFN3*3 20L-0.75
LKS32MC035DL6S8	48	32	4	6	8BITx1	2	4	1	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	SOP16L
LKS32MC035DL6S8B	48	32	4	5	8BITx1	2	4	1	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	SOP16L
LKS32MC035DL6S8C	48	32	4	5	8BITx1	2	4	1	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	SOP16L
LKS32MC035EL6S8B	48	32	4	5	8BITx1	2	4	1	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	5.7-28		5V LDO	SOP16L
LKS32MC035EL6S8C	48	32	4	5	8BITx1	2	4	1	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	5.7-28		5V LDO	SOP16L
LKS32MC037EM6S8	48	32	4	9	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	SSOP24L
LKS32MC037EM6S8B	48	32	4	9	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	SSOP24L
LKS32MC037EM6S8C	48	32	4	9	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	SSOP24L
LKS32MC037FM6S8B	48	32	4	8	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	5.7-28		5V LDO	SSOP24L
LKS32MC037FM6S8C	48	32	4	8	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	5.7-28		5V LDO	SSOP24L
LKS32MC037QM6Q8	48	32	4	9	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	QFN4*4 24L-0.75
LKS32MC037QM6Q8B	48	32	4	9	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	QFN4*4 24L-0.75
LKS32MC037QM6Q8C	48	32	4	9	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	QFN4*4 24L-0.75
LKS32MC037Q2M6Q8C	48	32	4	9	8BITx1	2	7	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	5.7-28		5V LDO	QFN4*4 24L-0.75
LKS32MC039DK6Q8B	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	QFN4*4 32L-0.75

LKS32MC039DK6Q8C	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes	3P3N	+0.05/-0.3	7.5-28		5V LDO	QFN4*4 32L-0.75
LKS32MC039PL5K6Q8B*	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes					5V LDO	QFN5*5 32L-0.75
LKS32MC039PL5K6Q8C*	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes					5V LDO	QFN5*5 32L-0.75
LKS32MC039PL3K6Q8B	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes					3.3V LDO	QFN4*4 32L-0.75
LKS32MC039PL3K6Q8C	48	32	4	9	8BITx1	2	8	2	3	1	1	1	Yes	Yes					3.3V LDO	QFN4*4 32L-0.75

* LKS32MC039PL5K6Q8B/LKS32MC039PL3K6Q8B integrate a three-phase full bridge circuit composed of three pairs of MOS.

2.1 System Resources

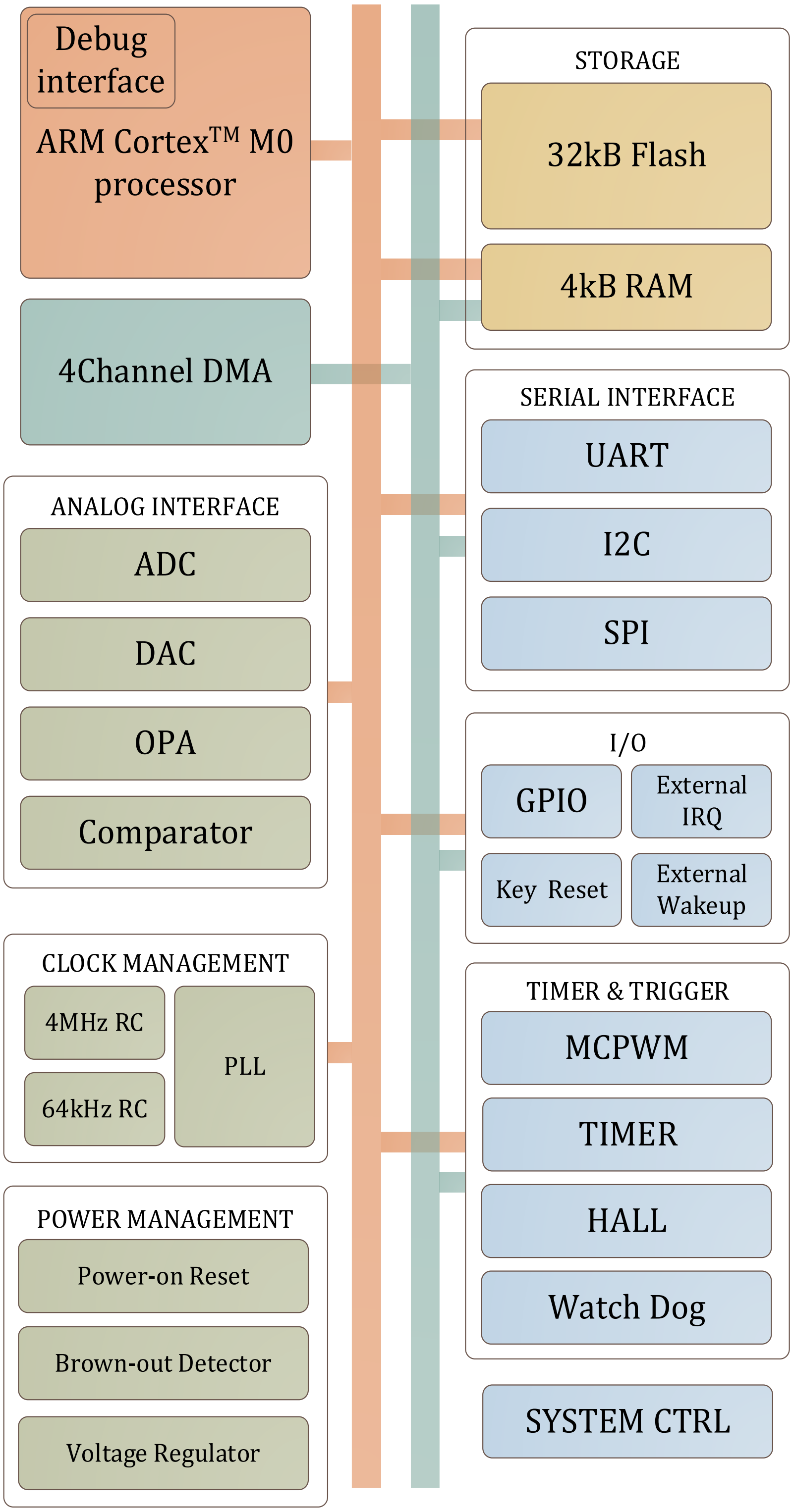

Figure 2-1 LKS32MC03x System Block Diagram

2.2 FOC System

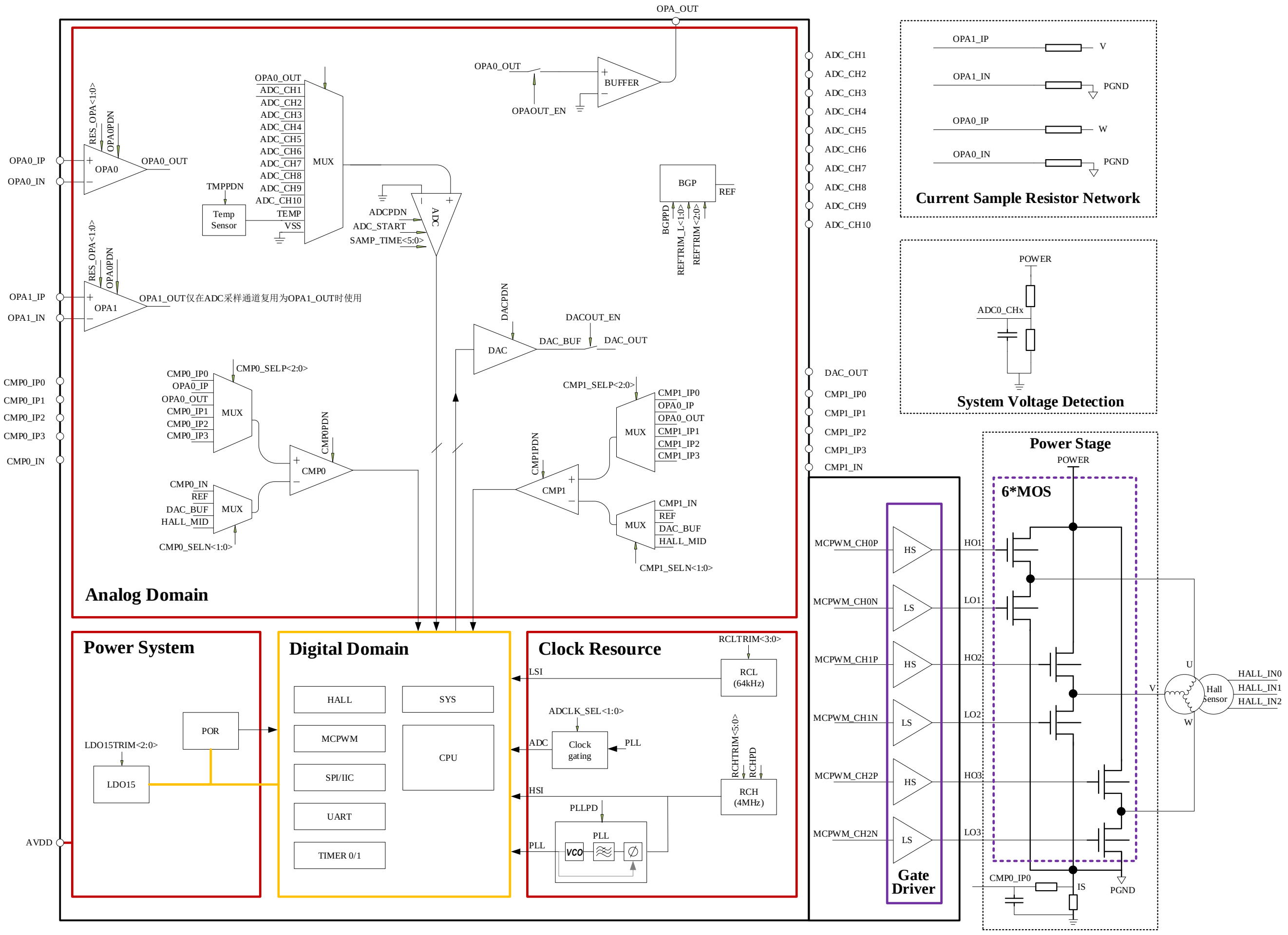

Figure 2-2 Simplified Schematic Diagram of the LKS32MC03x Vector Sinusoidal Control System

3 Pin Assignment

3.1 Pin Assignment Diagram

3.1.1 Special Notes

PU is short for pull-up. The PU pin in the following pin diagrams is designed with an internal pull-up resistor to the AVDD.

The RSTN pin is equipped with an internal 100kΩ pull-up resistor that is fixed to turn on the pull-up, which can be turned off when the RSTN function is switched to the GPIO function

The SWDIO/SWCLK comes with an internal 10kΩ pull-up resistor that is fixed to turn on the pull-up, which can be turned off when the SWD function is switched to the GPIO function

The remaining PU pins have an internal 10kΩ pull-up resistor that can be turned on or off by software control.

EXTI is external interrupt or GPIO interrupt input pin.

WK is short for wake-up, is external wake-up source.

UARTx_TX(RX): UART supports an interchange between the TX and RX. When the second function of GPIO is selected as UART and GPIO_PIE i.e. input is enabled, it can be used as UART_RX; When GPIO_POE is enabled, it can be used as UART_TX. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

SPI_DI(DO): The DI and DO of SPI can be interchanged. When the second function of GPIO is SPI, and GPIO_PIE i.e. input is enabled, it can be used as SPI_DI; when GPIO_POE i.e. output is enabled, it can be used as SPI_DO. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

3.1.2 Version Difference

There are two versions for each package. The major difference is the pin location of ADC_CH6/ADC_CH7. For details, please refer to the table below.

C version is recommended for new design.

Table 3-1 Version Comparison

A Version		B/C Version	
DAC output range 0~3V		B Version: DAC output range0~3V/4.8V C Version: DAC output range0~1.2V/3V/4.8V	
P0_9	CLKO	P0_9	CLKO
	MCPWM_CH0P		MCPWM_CH0P
	UART0_RXD		UART0_RXD
	SPI_DO		SPI_DO
	SDA		SDA

	TIM0_CH1		TIM0_CH1
	ADC_TRIGGER		ADC_TRIGGER
	CMP0_IN		CMP0_IN
	PU		PU
	EXTI7		EXTI7
			ADC_CH6
	WK3		WK3
P0_10	CLKO	P0_10	CLKO
	MCPWM_CH0P		MCPWM_CH0P
	TIM0_CH0		TIM0_CH0
	TIM1_CH0		TIM1_CH0
	ADC_CH6		
	WK4		WK4
P0_15	MCPWM_CH2N	P0_15	MCPWM_CH2N
	TIM1_CH0		TIM1_CH0
	ADC_CH7		
	EXTI9		EXTI9
P1_6	CMP1_OUT	P1_6	CMP1_OUT
	HALL_IN1		HALL_IN1
	MCPWM_CH2N		MCPWM_CH2N
	UART0_TXD		UART0_TXD
	TIM0_CH1		TIM0_CH1
	ADC_TRIGGER		ADC_TRIGGER
			ADC_CH7
	CMP1_IP2		CMP1_IP2
	PU		PU
	EXTI12		EXTI12
P1_5	SPI_DI	P1_5	SPI_DI
	SCL		SCL
	TIM1_CH1		TIM1_CH1
	OPA1_IN		OPA1_IN
			ADC_CH8
	CMP1_IP0		CMP1_IP0
	PU		PU
	EXTI11		EXTI11
	WK5		WK5

In A Version, the chip doesn't have ADC_CH8 pin. In B Version, users who don't need OPA1, could use ADC_CH8 by setting SYS_OPA_SEL=0.

The chip contains an 8 bit DAC with an output signal range of 3 V for version A, 3 V/4.8 V for version B, and 1.2 V/3 V/4.8 V for version C.C chip, the SYS_AFE_REG2.BIT15 = 1 needs to be set to use the 1.2 V scale of the DAC.

By reading SYS_ AFE_ INFO.Version can view the chip version. 1 represents version A and 2 represents version B and 3 represents version C.

3.1.3 LKS32MC031PC6Q8C

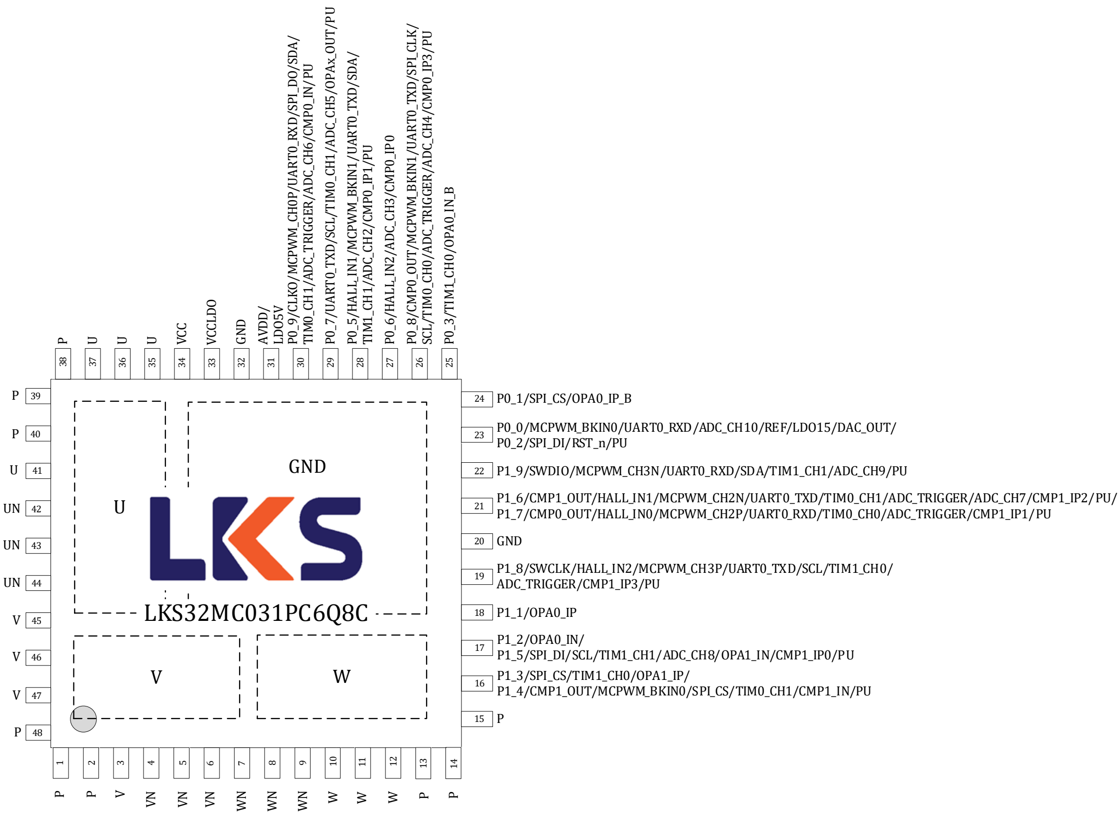

Figure 3-1 LKS32MC031PC6Q8BC Pin Assignment Diagram

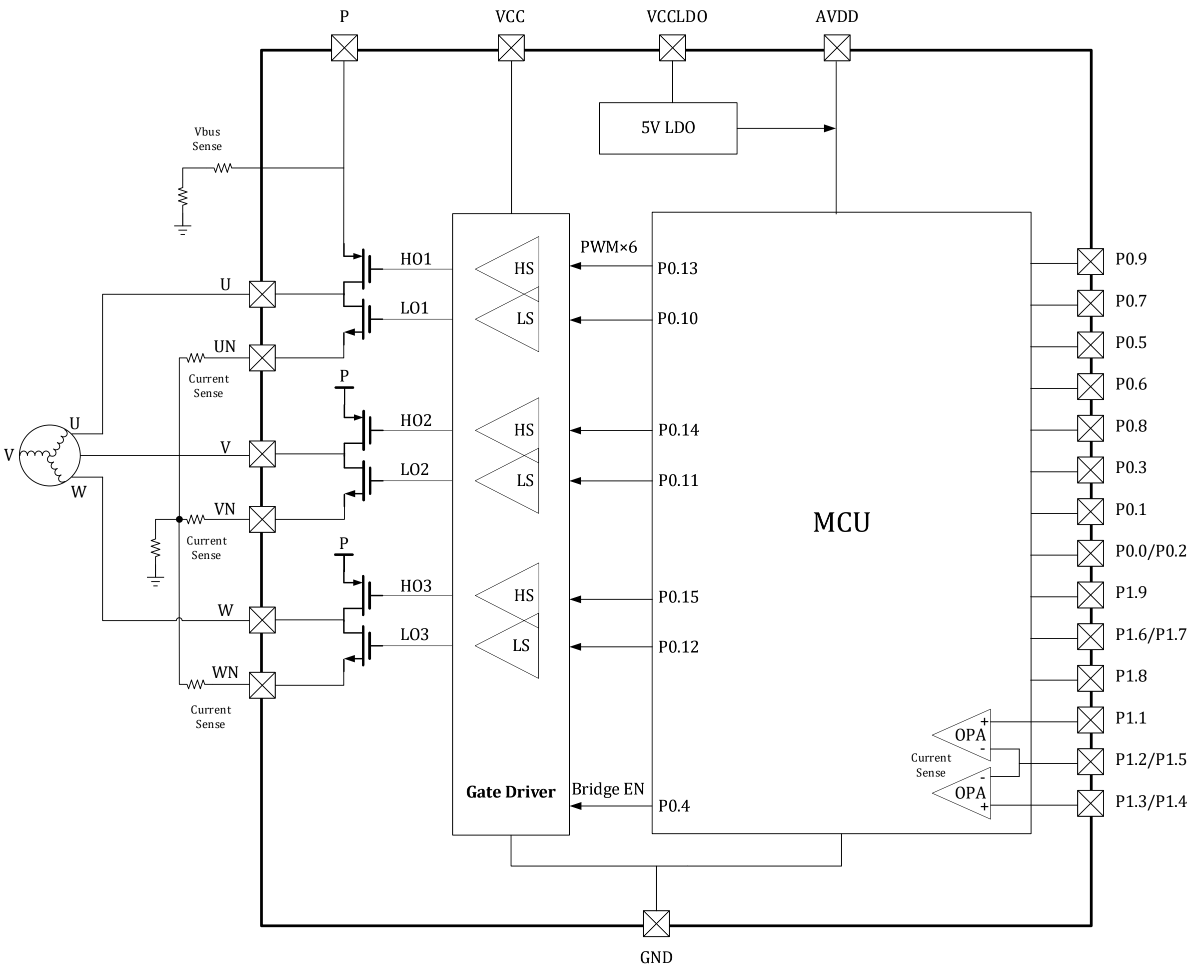

Figure 3-2 Schematic diagram of the LKS32MC031KLC6T8B(C) gate driver connection

Table 3-2 LKS32MC035DL6S8 Pin Description

0-U	U	Bottom U-phase output terminal connected with pin U
0-V	V	Bottom V-phase output terminal connected with pin V
0-W	W	Bottom W-phase output terminal connected with pin W
0-GND	GND	Bottom chip ground. It is strongly recommended that multiple ground pins be grounded uniformly on the PCB.
1	P	MOS Power Input
2	P	MOS Power Input
3	V	output for V phase
4	VN	V-phase lower arm N-mos source terminal
5	VN	V-phase lower arm N-mos source terminal
6	VN	V-phase lower arm N-mos source terminal
7	WN	W-phase lower arm N-mos source terminal
8	WN	W-phase lower arm N-mos source terminal
9	WN	W-phase lower arm N-mos source terminal
10	W	output for W phase
11	W	output for W phase

12	W	output for W phase
13	P	MOS Power Input
14	P	MOS Power Input
15	P	MOS Power Input
16	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	QEP1_CH0	
	QEP1_CH0	
	OPA1_IP	OPA1 positive input
	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	QEP0_CH1	
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
17	P1_2	P1.2
	OPA0_IN	OPA0 negative input
	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	QEP1_CH1	
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
18	P1_1	P1.1
	OPA0_IP	OPA0 positive input
19	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	QEP1_CH0	
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
20	GND	Ground

21	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	QEP0_CH1	
	QEP0_CH1	
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	QEP0_CH0	
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
22	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	QEP1_CH1	
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
23	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be

		100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
24	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
25	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	QEP1_CH0	
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
26	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	QEP0_CH0	
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
27	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
28	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	QEP1_CH1	
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
29	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	QEP0_CH1	
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software

30	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	QEP0_CH1	
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
31	AVDD	Power supply, 2.2~5.5V
	LDO15	1.5V LDO output
32	GND	Ground
33	VCCLDO	5V LDO power input
34	VCC	Gate-drive power input
35	U	output for U phase
36	U	output for U phase
37	U	output for U phase
38	P	MOS Power Input
39	P	MOS Power Input
40	P	MOS Power Input
41	NC	Not connected
42	UN	U-phase lower arm N-mos drain terminal
43	UN	U-phase lower arm N-mos drain terminal
44	UN	U-phase lower arm N-mos drain terminal
45	V	output for V phase
46	V	output for V phase
47	V	output for V phase
48	P	MOS Power Input

3.1.4 LKS32MC033PH6Q8C

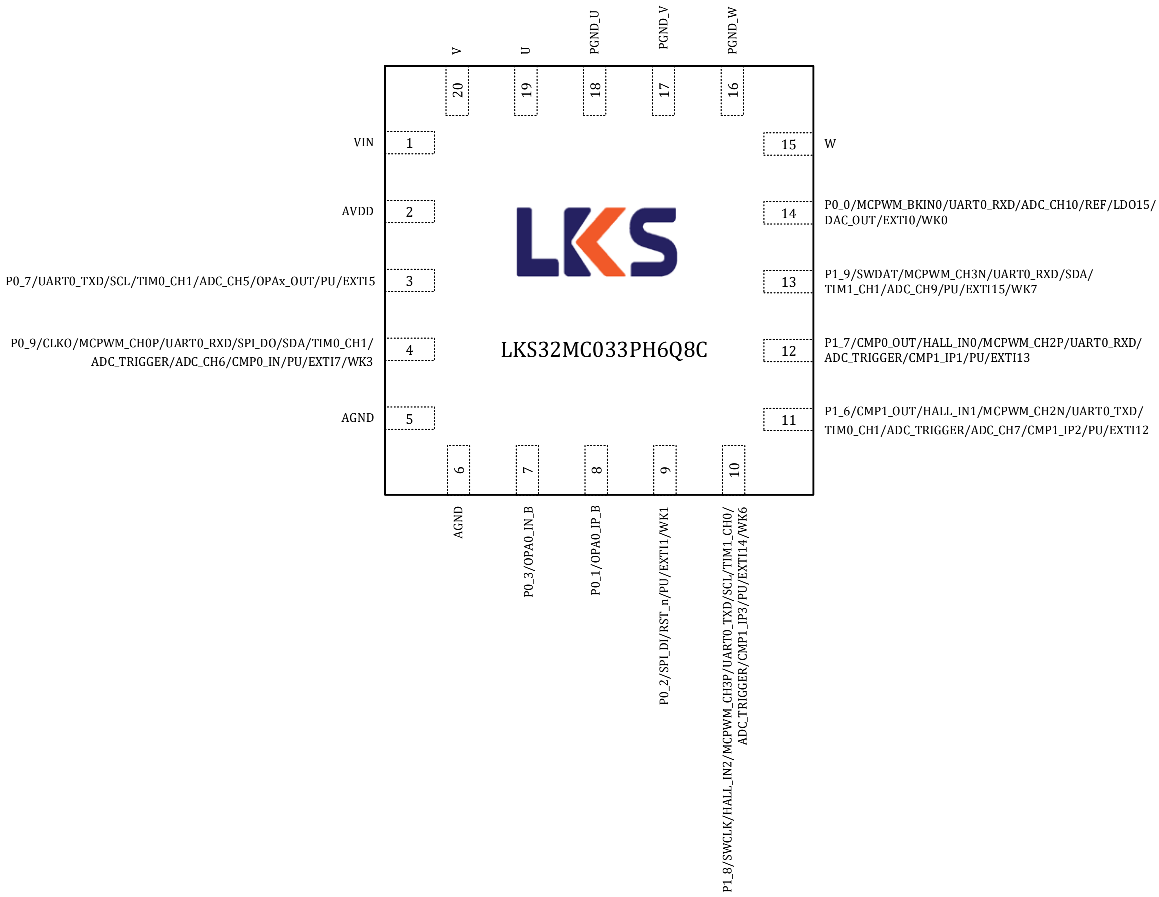

Figure 3-3 LKS32MC033PH6Q8C Pin Assignment Diagram

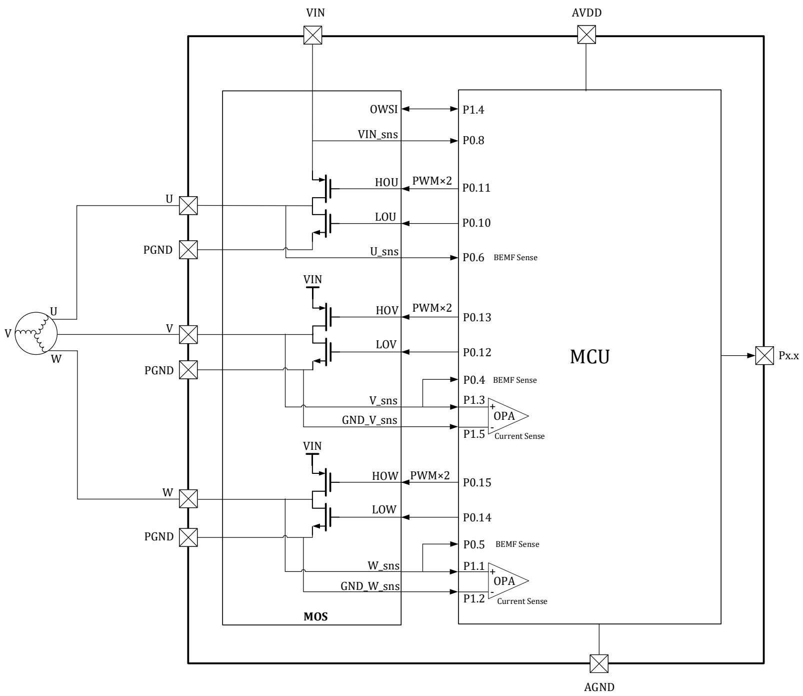

Figure 3-4 Schematic diagram of the LKS32MC033PH6Q8C gate driver connection

Table 3-3 LKS32MC033PH6Q8 Pin Description

1	VIN	芯片电源，供电范围 2.8~5.5V
2	AVDD	芯片电源，供电范围 2.5~5.5V
3	P0_7	P0.7
	UART0_TXD	串口 0 发送(接收)
	SCL	I2C 时钟
	TIM0_CH1	Timer0 通道 1
	ADC_CH5	ADC 通道 5
	OPAx_OUT	运放输出
	PU	内置 10kΩ 上拉电阻，软件可关闭
	EXTI5	外部 GPIO 中断信号 5
4	P0_9	P0.9
	CLKO	时钟输出(用于调试)
	MCPWM_CH0P	PWM 通道 0 高边
	UART0_RXD	串口 0 接收(发送)
	SPI_DO	SPI 数据输出(输入）
	SDA	I2C 数据
	TIM0_CH1	Timer0 通道 1
	ADC_TRIGGER	ADC 触发信号输出(用于调试)
	ADC_CH6	ADC 通道 6
	CMP0_IN	比较器 0 负端输入

	PU	内置 10kΩ 上拉电阻，软件可关闭
	EXTI7	外部 GPIO 中断信号 7
	WK3	外部唤醒信号 3
5	AGND	模拟地
6	AGND	模拟地
7	P0_3	P0.3
	OPA0_IN_B	运放 0 负端输入 B,请留意：OPA0 有两组输入信号，如果需要使用 B 组输入，需要设置 SYS_AFE_REG0[5] = 1。
8	P0_1	P0.1
	OPA0_IP_B	运放 0 正端输入 B,请留意：OPA0 有两组输入信号，如果需要使用 B 组输入，需要设置 SYS_AFE_REG0[5] = 1。
9	P0_2	P0.2
	SPI_DI	SPI 数据输入(输出）
	RST_n	复位引脚，P0.2 默认用作 RSTN。 建议接一个 10nF~100nF 的电容到地，并在 RSTN 和 AVDD 之间放置一个 10k~20k 的上拉电阻。 如果外部有上拉电阻，RSTN 的电容应为 100nF。P0.2 可切换为 GPIO，切换后可关闭 10kΩ 上拉电阻。
	PU	内置 10kΩ 上拉电阻，软件可关闭
	EXTI1	外部 GPIO 中断信号 1
	WK1	外部唤醒信号 1
10	P1_8	P1.8
	SWCLK	SWD 时钟
	HALL_IN2	HALL 接口输入 2
	MCPWM_CH3P	PWM 通道 3 高边
	UART0_TXD	串口 0 发送(接收)
	SCL	I2C 时钟
	TIM1_CH0	Timer1 通道 0
	ADC_TRIGGER	ADC 触发信号输出(用于调试)
	CMP1_IP3	比较器 1 正端输入 3
	PU	内置 10kΩ 上拉电阻，软件可关闭
	EXTI14	外部 GPIO 中断信号 14
	WK6	外部唤醒信号 6
11	P1_6	P1.6
	CMP1_OUT	比较器 1 输出
	HALL_IN1	HALL 接口输入 1
	MCPWM_CH2N	PWM 通道 2 低边
	UART0_TXD	串口 0 发送(接收)
	TIM0_CH1	Timer0 通道 1
	ADC_TRIGGER	ADC 触发信号输出(用于调试)
	CMP1_IP2	比较器 1 正端输入 2
	PU	内置 10kΩ 上拉电阻，软件可关闭
	EXTI12	外部 GPIO 中断信号 12

12	P1_7	P1.7
	CMP0_OUT	比较器 0 输出
	HALL_IN0	HALL 接口输入 0
	MCPWM_CH2P	PWM 通道 2 高边
	UART0_RXD	串口 0 接收(发送)
	ADC_TRIGGER	ADC 触发信号输出(用于调试)
	CMP1_IP1	比较器 1 正端输入 1
	PU	内置 10kΩ 上拉电阻，软件可关闭
	EXTI13	外部 GPIO 中断信号 13
13	P1_9	P1.9
	SWDAT	SWD 数据
	MCPWM_CH3N	PWM 通道 3 低边
	UART0_RXD	串口 0 接收(发送)
	SDA	I2C 数据
	TIM1_CH1	Timer1 通道 1
	ADC_CH9	ADC 通道 9
	PU	内置 10kΩ 上拉电阻，软件可关闭
	EXTI15	外部 GPIO 中断信号 15
	WK7	外部唤醒信号 7
14	P0_0	P0.0
	MCPWM_BKIN0	PWM 停机输入信号 0
	UART0_RXD	串口 0 接收(发送)
	ADC_CH10	ADC 通道 10
	REF	参考电压
	DAC_OUT	DAC 输出
	EXTI0	外部 GPIO 中断信号 0
	WK0	外部唤醒信号 0
15	W	W 相输出端
16	PGND_W	W 相功率地
17	PGND_V	V 相功率地
18	PGND_U	U 相功率地
19	U	U 相输出端
20	V	V 相输出端

*P/N MOS 信息详见第五章电气性能

3.1.5 LKS32MC035DL6S8

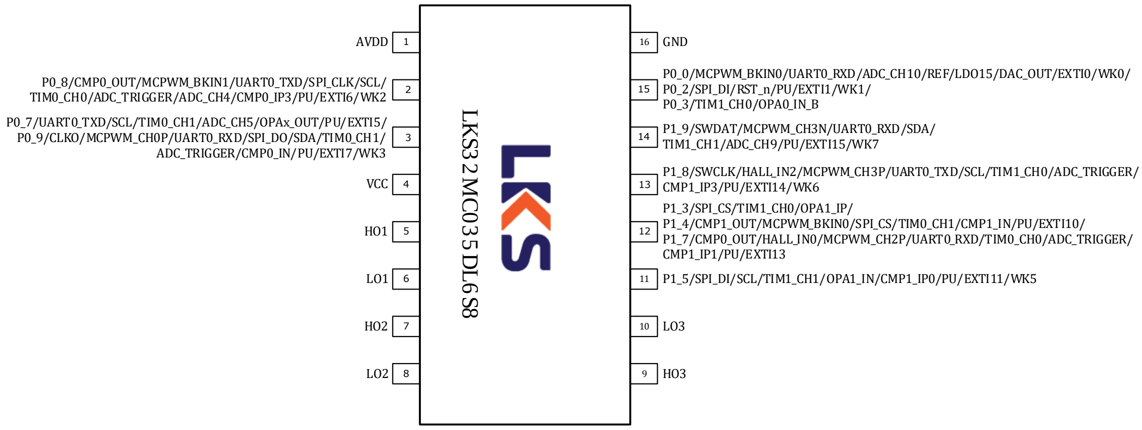

Figure 3-5 LKS32MC035DL6S8 Pin Assignment Diagram

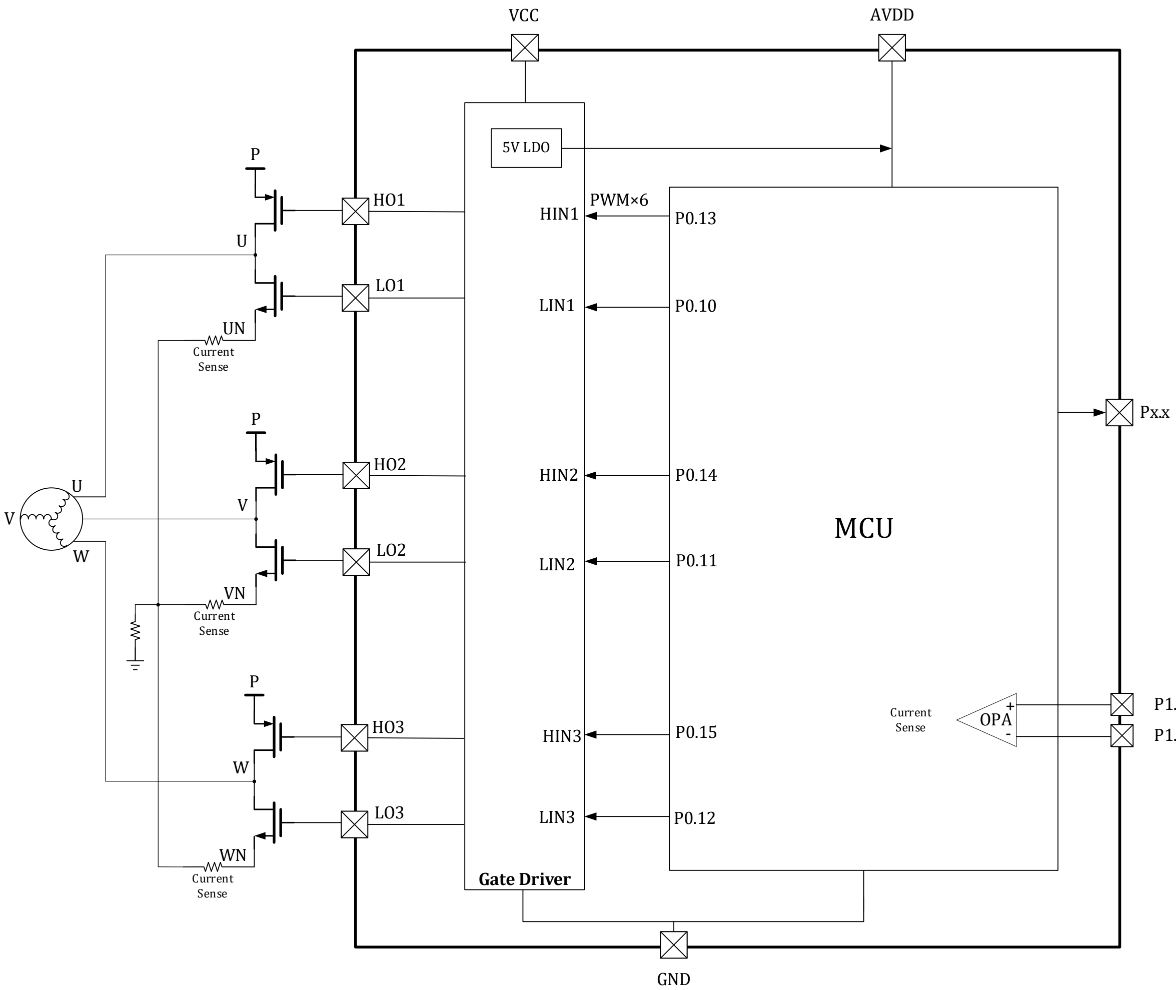

Figure 3-6 Schematic diagram of the LKS32MC035DL6S8 gate driver connection

Table 3-4 LKS32MC035DL6S8 Pin Description

1	AVDD	5V LDO output, an external 1uF decoupling capacitor as close as possible to the LDO5V pin

		is recommended.
2	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
3	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
4	VCC	For 035D, this pin is power supply. If VCC is higher than 20V, the AVDD pin is powered by the LDO5V output of the chip. It is recommended to add a shunt resistance of 1k-2k ohm between the VCC and AVDD. Refer to Chapter 7 for specific resistance calculations. There must be a decoupling capacitor higher than or equal to 1uF between the VCC pin and the ground.
5	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
6	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of

		P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
7	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
8	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
9	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
10	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
11	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
12	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
13	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2

	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
14	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
15	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
16	GND	Ground

3.1.6 LKS32MC035DL6S8B/ LKS32MC035DL6S8C

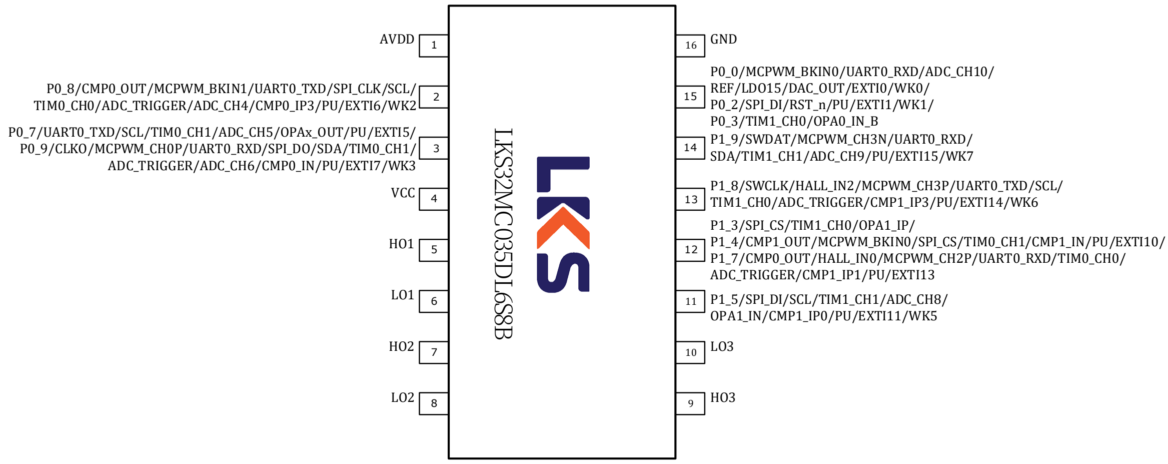

Figure 3-7 LKS32MC035DL6S8B(C) Pin Assignment Diagram

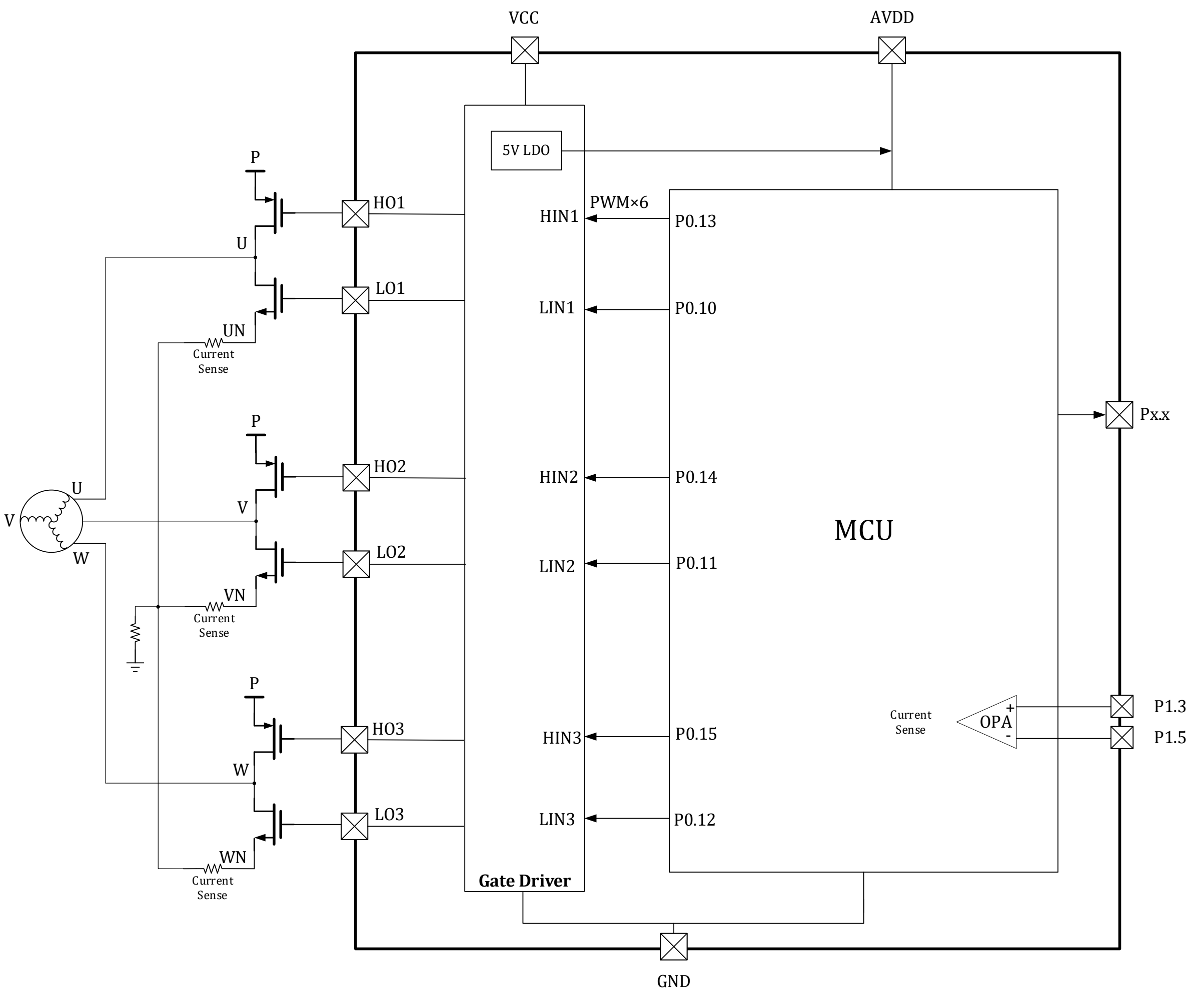

Figure 3-8 Schematic diagram of the LKS32MC035DL6S8B(C) gate driver connection

Table 3-5 LKS32MC035DL6S8B(C) Pin Description

1	AVDD	5V LDO output, an external 1uF decoupling capacitor as close as possible to the LDO5V pin is recommended.
2	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
3	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
4	VCC	For 035D, this pin is power supply. If VCC is higher than 20V, the AVDD pin is powered by the LDO5V output of the chip. It is recommended to add a shunt resistance of 1k-2k ohm between the VCC and AVDD. Refer to Chapter 7 for specific resistance calculations. There must be a decoupling capacitor higher than or equal to 1uF between the VCC pin and the ground.
5	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of

		P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
6	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
7	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
8	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
9	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
10	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
11	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
12	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13

13	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
14	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
15	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1

16	GND	Ground

3.1.7 LKS32MC035EL6S8B/ LKS32MC035EL6S8C

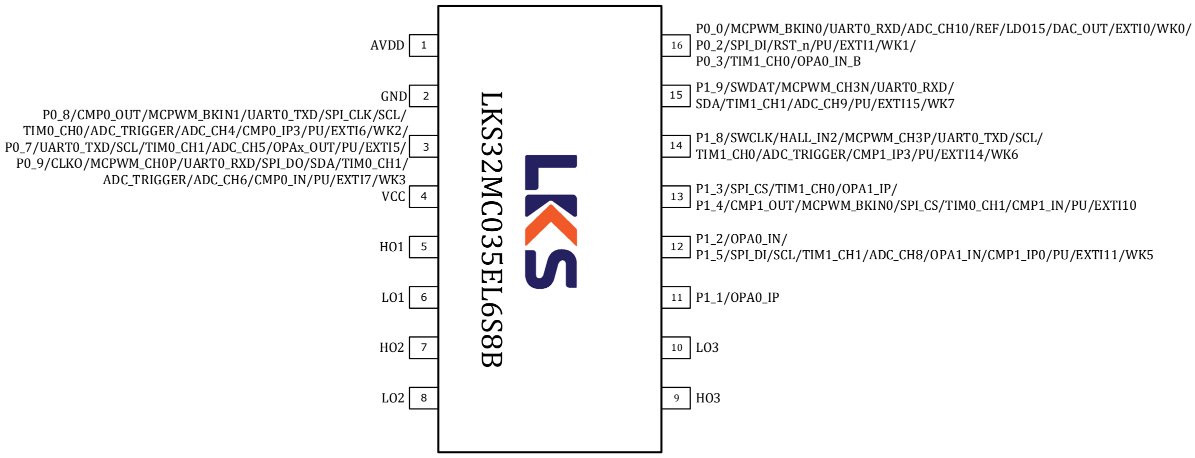

Figure 3-9 LKS32MC035EL6S8B(C) Pin Assignment Diagram

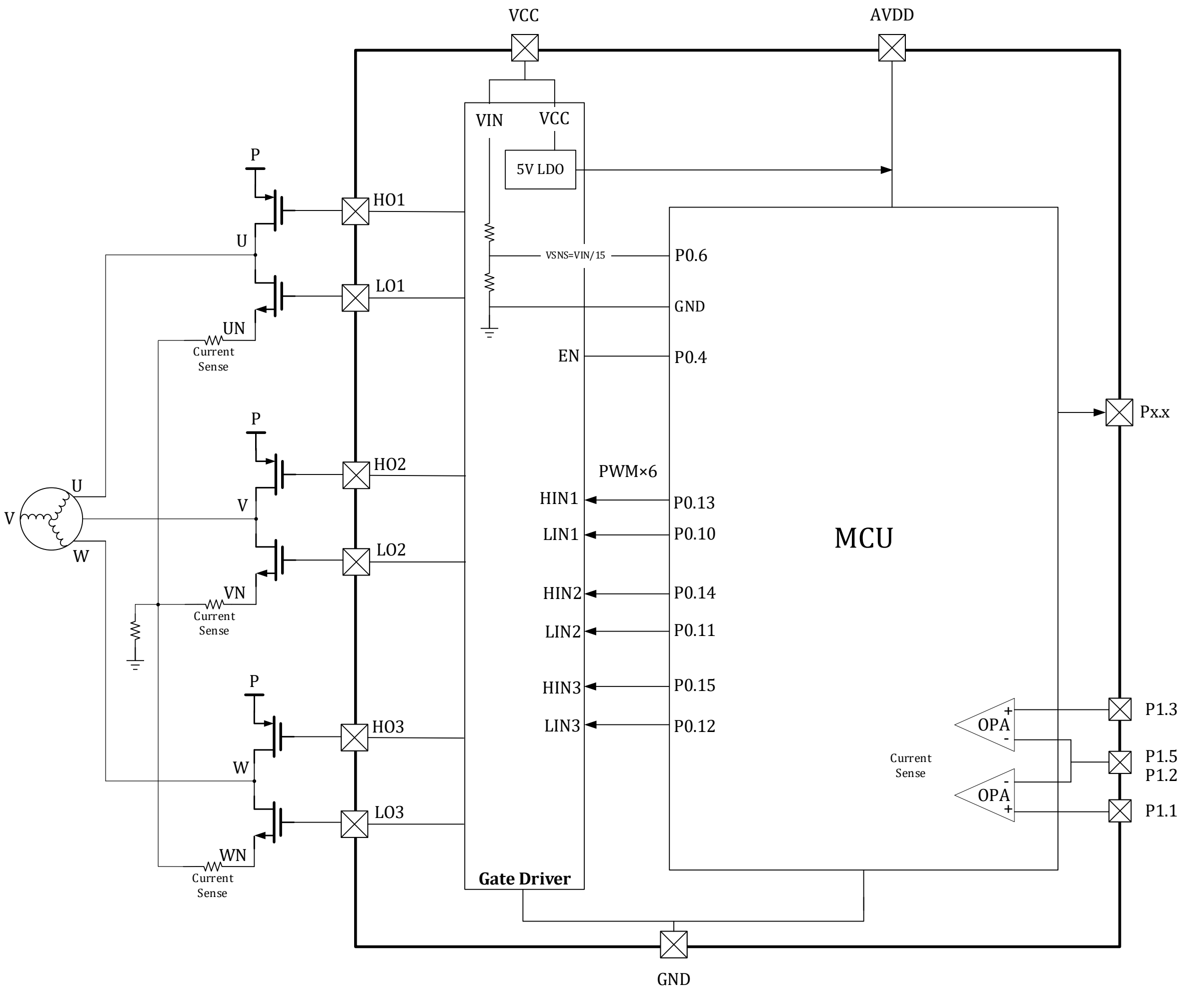

Figure 3-10 Schematic diagram of the LKS32MC035EL6S8B(C) gate driver connection

Table 3-6 LKS32MC035EL6S8B(C) Pin Description

1	AVDD	Power supply, 2.2~5.5V
2	GND	Ground
3	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
4	VCC	Gate driver power supply
5	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
6	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
7	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as

		that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
8	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
9	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
10	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
11	P1_1	P1.1
	OPA0_IP	OPA0 positive input
12	P1_2	P1.2
	OPA0_IN	OPA0 negative input
	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
13	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
14	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software

	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
15	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
16	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1

3.1.8 LKS32MC037EM6S8

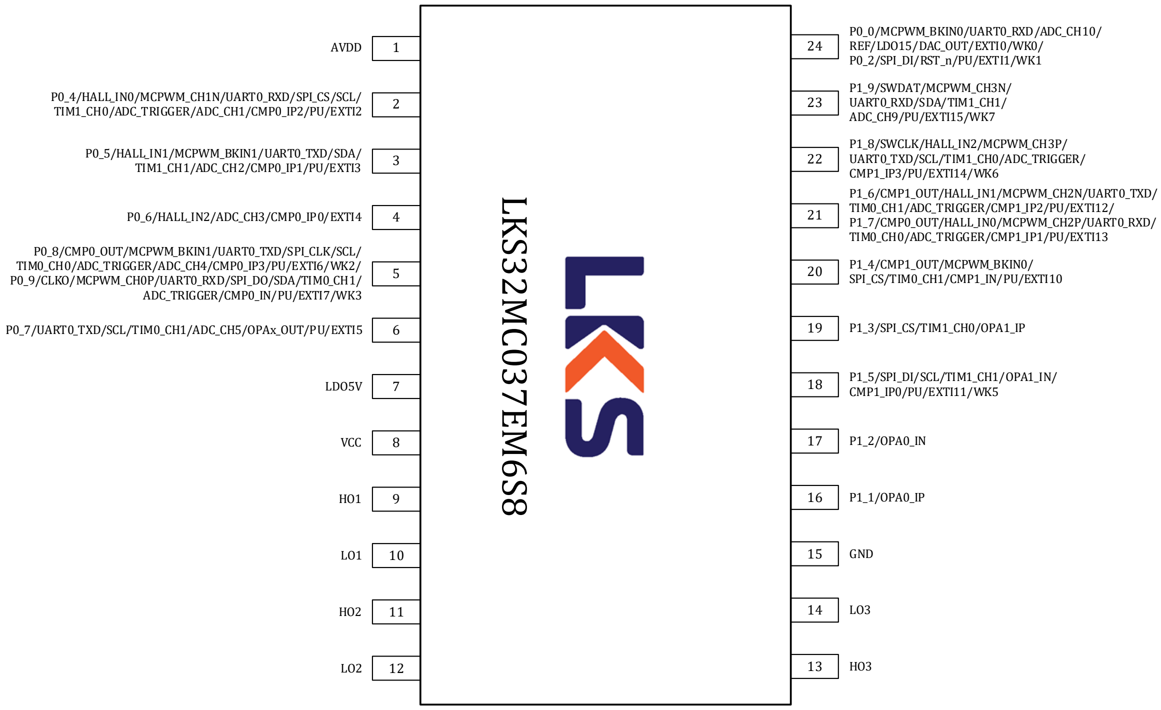

Figure 3-11 LKS32MC037EM6S8 Pin Assignment Diagram

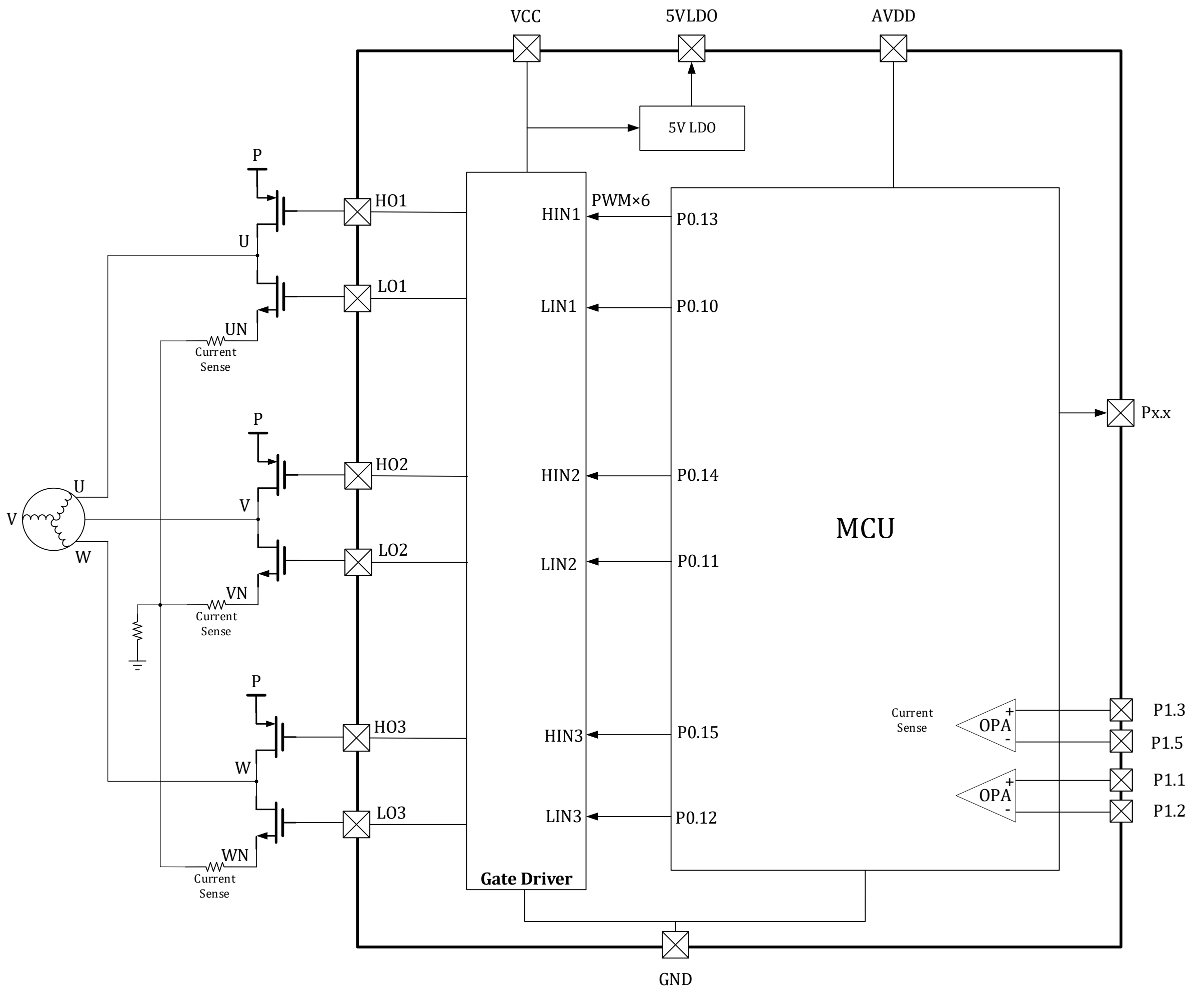

Figure 3-12 Schematic diagram of the LKS32MC037EM6S8 gate driver connection

Table 3-7 LKS32MC037EM6S8 Pin Description

1	AVDD	MCU low voltage power supply, should be 2.5-5.5V. In applications with good heat dissipation conditions, it can be directly connected to the 5V LDO pin of the chip. Connect this pin to an external 5V power supply if you are considering reducing the system power consumption using a 5V power supply generated by an external DCDC or charge pump.
2	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2

3	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
4	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
5	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
6	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock

	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
7	LDO5V	5V LDO output. It is recommended to connect an external 1uF decoupling capacitor, as close as possible to the LDO5V pin.
8	VCC	This pin is power supply. If VCC is higher than 20V, the AVDD pin is powered by the LDO5V output of the chip. It is recommended to add a shunt resistance of 1k-2k ohm between the VCC and AVDD. Refer to Chapter 7 for specific resistance calculations. There must be a decoupling capacitor higher than or equal to 1uF between the VCC pin and the ground.
9	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
10	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
11	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
12	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
13	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
14	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
15	GND	Ground
16	P1_1	P1.1
	OPA0_IP	OPA0 positive input
17	P1_2	P1.2
	OPA0_IN	OPA0 negative input
18	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
19	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
20	P1_4	P1.4

	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
21	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12
	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
22	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
23	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side

	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
24	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1

3.1.9 LKS32MC037EM6S8B/ LKS32MC037EM6S8C

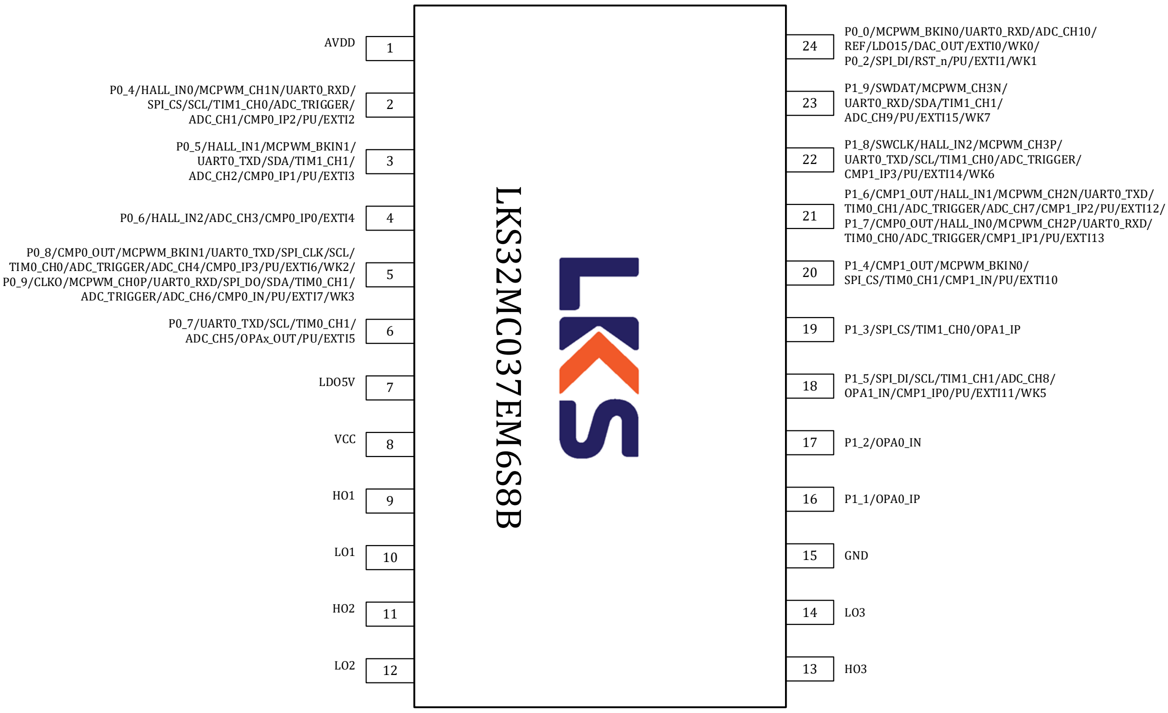

Figure 3-13 LKS32MC037EM6S8B(C) Pin Assignment Diagram

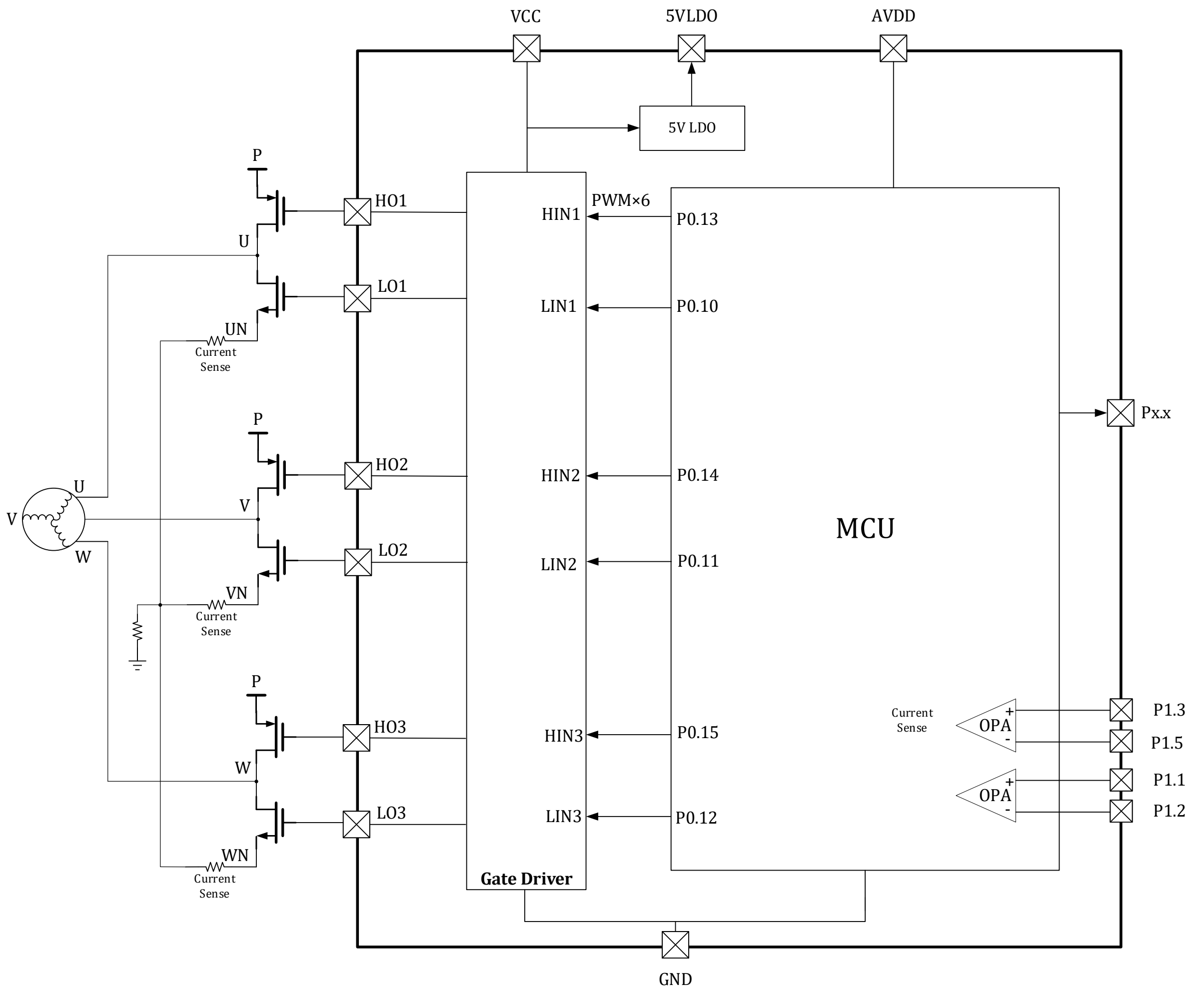

Figure 3-14 Schematic diagram of the LKS32MC037EM6S8B(C) gate driver connection

Table 3-8 LKS32MC037EM6S8B(C) Pin Description

1	AVDD	MCU low voltage power supply, should be 2.5-5.5V. In applications with good heat dissipation conditions, it can be directly connected to the 5V LDO pin of the chip. Connect this pin to an external 5V power supply if you are considering reducing the system power consumption using a 5V power supply generated by an external DCDC or charge pump.
2	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2

3	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
4	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
5	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
6	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)

	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
7	LDO5V	5V LDO output. It is recommended to connect an external 1uF decoupling capacitor, as close as possible to the LDO5V pin.
8	VCC	This pin is power supply. If VCC is higher than 20V, the AVDD pin is powered by the LDO5V output of the chip. It is recommended to add a shunt resistance of 1k-2k ohm between the VCC and AVDD. Refer to Chapter 7 for specific resistance calculations. There must be a decoupling capacitor higher than or equal to 1uF between the VCC pin and the ground.
9	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
10	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
11	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
12	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
13	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
14	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
15	GND	Ground
16	P1_1	P1.1
	OPA0_IP	OPA0 positive input
17	P1_2	P1.2
	OPA0_IN	OPA0 negative input
18	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
19	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0

	OPA1_IP	OPA1 positive input
20	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
21	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12
	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
22	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
23	P1_9	P1.9

	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
24	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1

3.1.10 LKS32MC037FM6S8B/ LKS32MC037FM6S8C

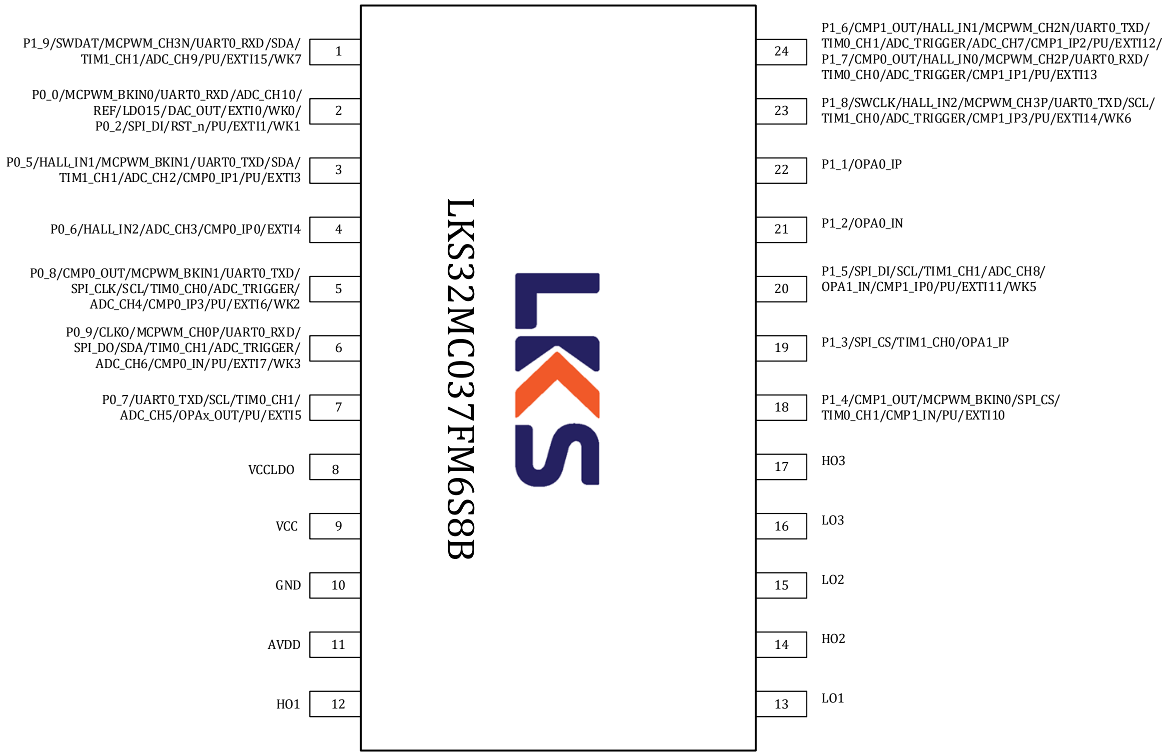

Figure 3-15 LKS32MC037FM6S8B(C) Pin Assignment Diagram

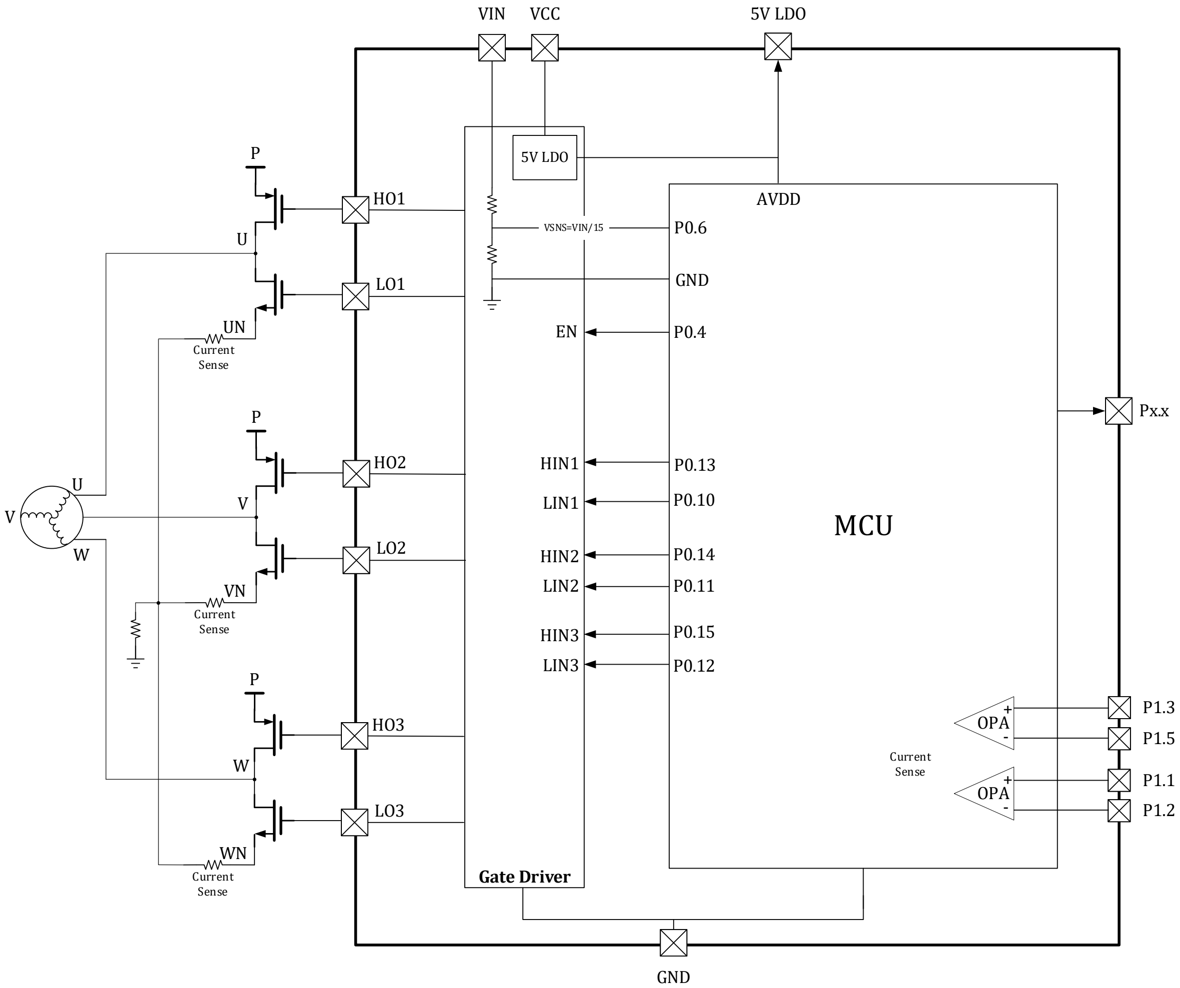

Figure 3-16 Schematic diagram of the LKS32MC037FM6S8B(C) gate driver connection

Table 3-9 LKS32MC037FM6S8B(C) Pin Description

1	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
2	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output

	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
3	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
4	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
5	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
6	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side

	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
7	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
8	VCCLDO	5V LDO power supply, 7-20 V, with an output current limit of < 80mA. Decoupling capacitors should be > 0.33uF and placed as close as possible to this pin.
9	VCC	Gate driver power supply
10	GND	Ground
11	AVDD	Power supply, 2.2~5.5V
12	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
13	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
14	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
15	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
16	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
17	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
18	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10

19	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
20	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
21	P1_2	P1.2
	OPA0_IN	OPA0 negative input
22	P1_1	P1.1
	OPA0_IP	OPA0 positive input
23	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
24	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12
	P1_7	P1.7
	CMP0_OUT	Comparator 0 output

	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13

3.1.11 LKS32MC037QM6Q8

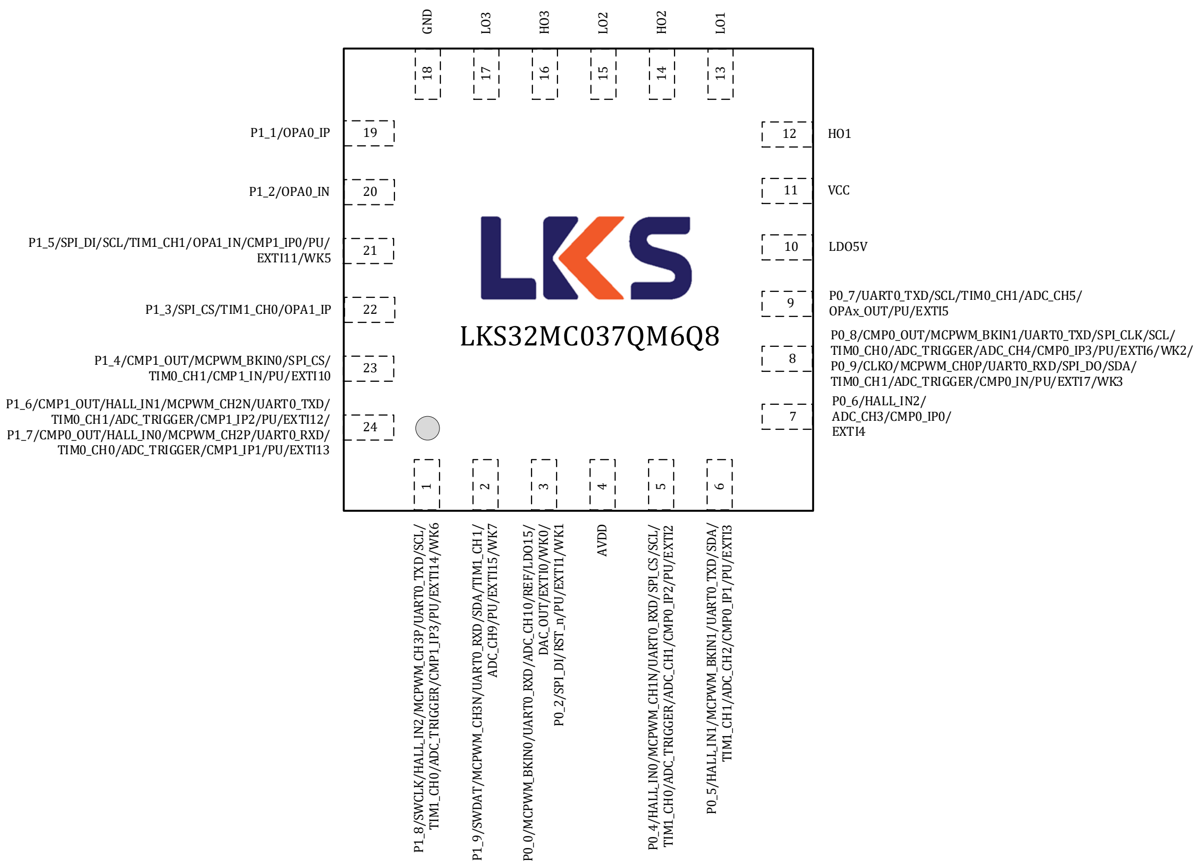

Figure 3-17 LKS32MC037QM6Q8 Pin Assignment Diagram

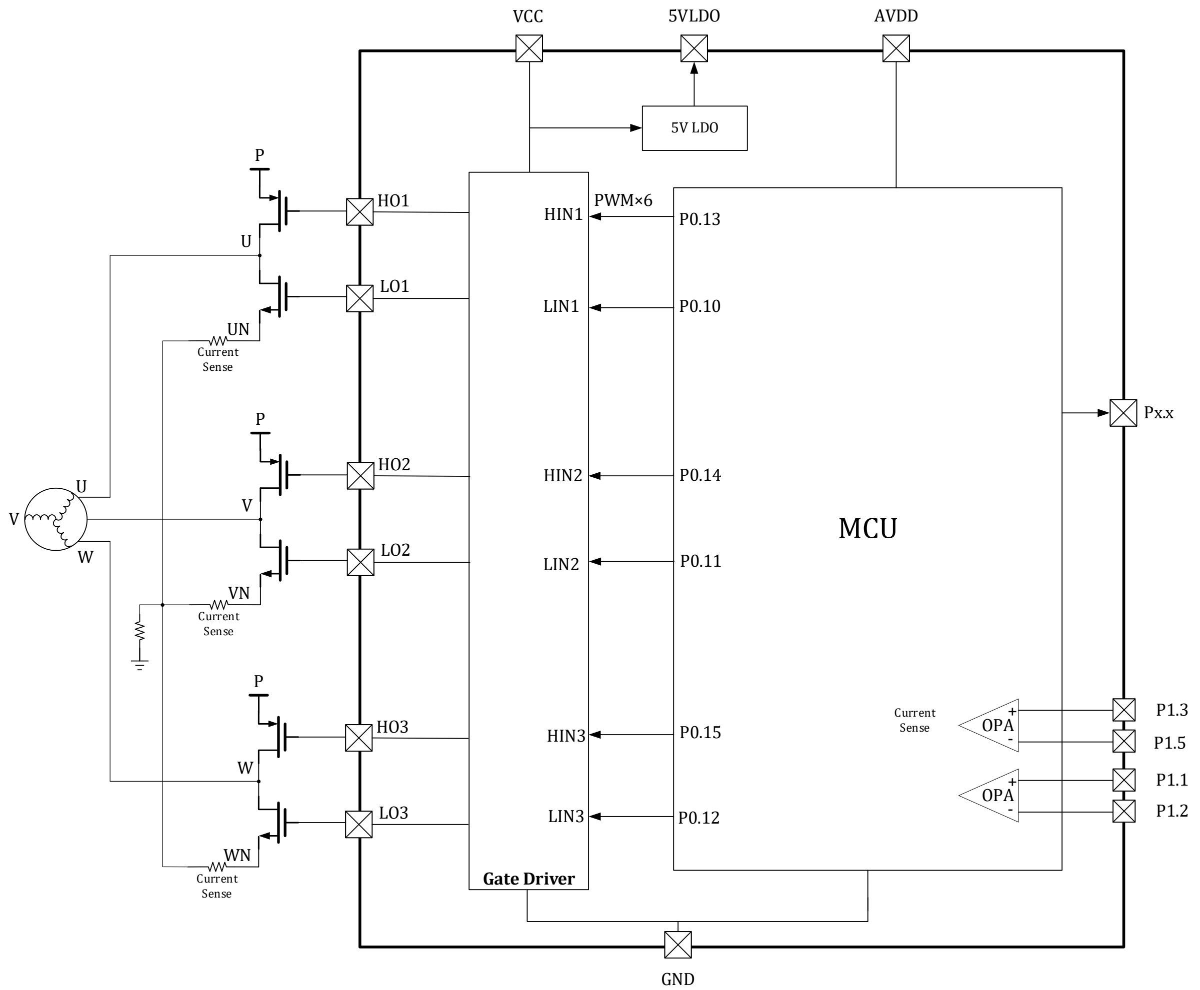

Figure 3-18 Schematic diagram of the LKS32MC037QM6Q8 gate driver connection

Table 3-10 LKS32MC037QM6Q8 Pin Description

0	GND	Ground in the belly of the chip
1	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
2	P1_9	P1.9
	SWDAT	SWD Data

	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
3	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
4	AVDD	MCU low voltage power supply, should be 2.5-5.5V. In applications with good heat dissipation conditions, it can be directly connected to the 5V LDO pin of the chip. Connect this pin to an external 5V power supply if you are considering reducing the system power consumption using a 5V power supply generated by an external DCDC or charge pump.
5	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2
6	P0_5	P0.5

	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
7	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
8	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
9	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1

	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
10	LDO5V	5V LDO output. It is recommended to connect an external 1uF decoupling capacitor, as close as possible to the LDO5V pin.
11	VCC	This pin is power supply. If VCC is higher than 20V, the AVDD pin is powered by the LDO5V output of the chip. It is recommended to add a shunt resistance of 1k-2k ohm between the VCC and AVDD. Refer to Chapter 7 for specific resistance calculations. There must be a decoupling capacitor higher than or equal to 100uF between the VCC pin and the ground.
12	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
13	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
14	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
15	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
16	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
17	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
18	GND	Ground
19	P1_1	P1.1
	OPA0_IP	OPA0 positive input
20	P1_2	P1.2
	OPA0_IN	OPA0 negative input
21	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
22	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
23	P1_4	P1.4
	CMP1_OUT	Comparator 1 output

	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
24	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12
	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13

3.1.12 LKS32MC037QM6Q8B/ LKS32MC037QM6Q8C/LKS32MC037Q2M6Q8C

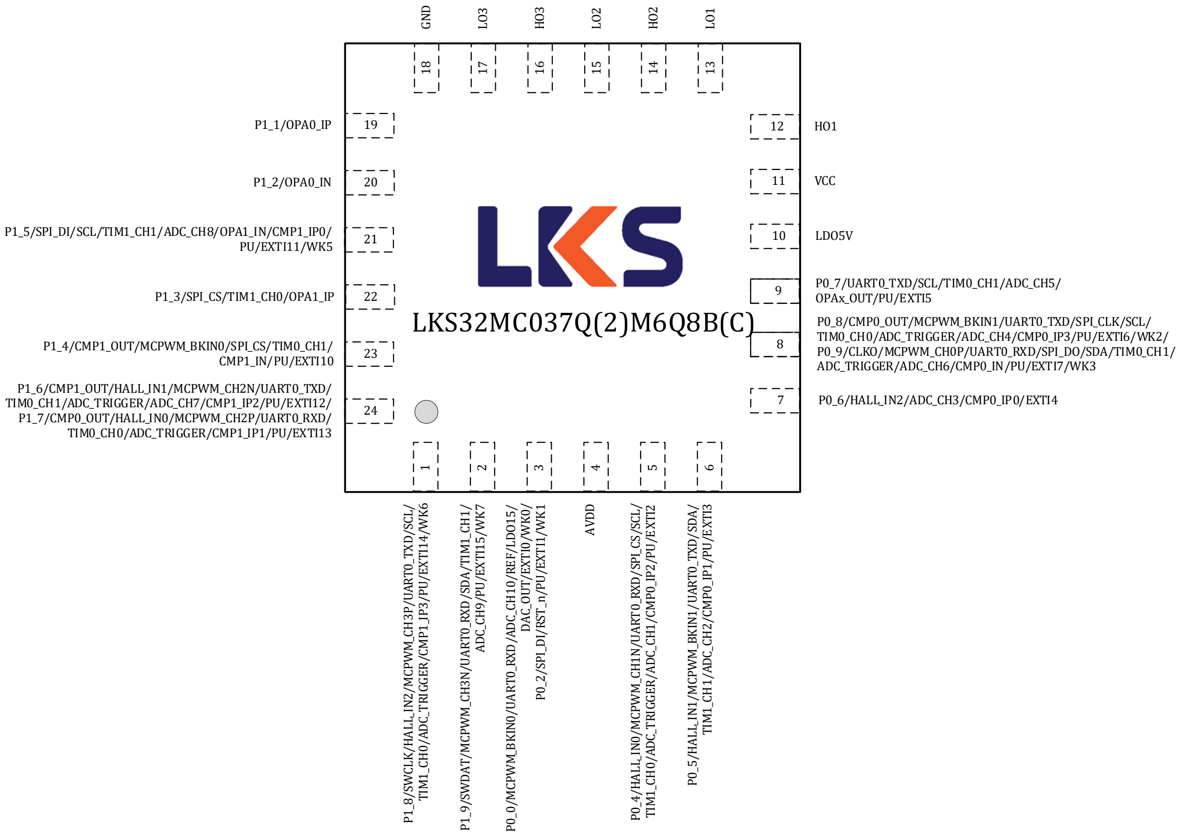

Figure 3-19 LKS32MC037QM6Q8B(C) Pin Assignment Diagram

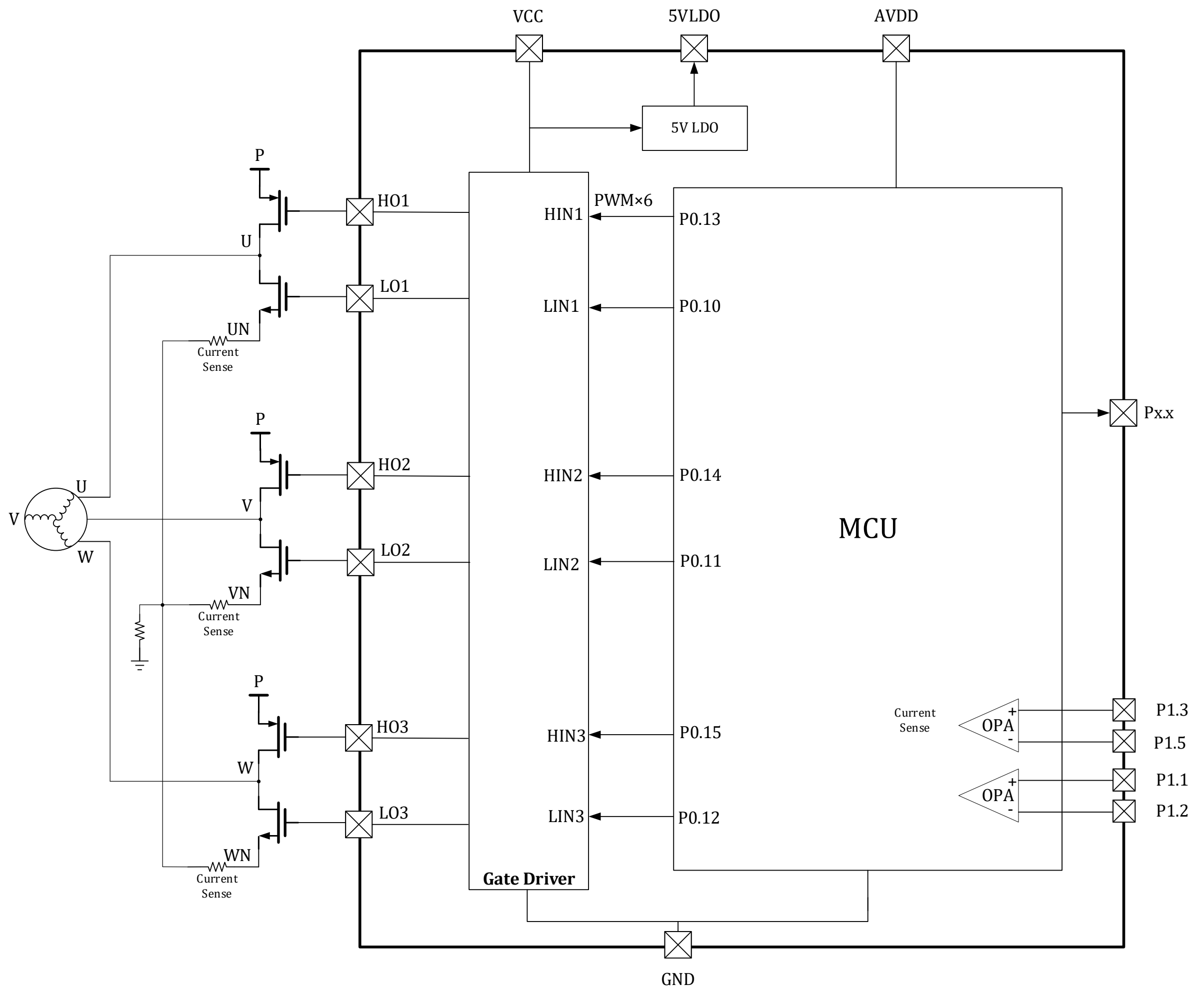

Figure 3-20 Schematic diagram of the LKS32MC037QM6Q8B(C) gate driver connection

Table 3-11 LKS32MC037QM6Q8B(C) Pin Description

0	GND	Ground in the belly of the chip
1	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
2	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side

	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
3	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
4	AVDD	MCU low voltage power supply, should be 2.5-5.5V. In applications with good heat dissipation conditions, it can be directly connected to the 5V LDO pin of the chip. Connect this pin to an external 5V power supply if you are considering reducing the system power consumption using a 5V power supply generated by an external DCDC or charge pump.
5	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2
6	P0_5	P0.5
	HALL_IN1	Hall interface input 1

	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
7	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
8	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
9	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1

	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
10	LDO5V	5V LDO output. It is recommended to connect an external 1uF decoupling capacitor, as close as possible to the LDO5V pin.
11	VCC	This pin is power supply. If VCC is higher than 20V, the AVDD pin is powered by the LDO5V output of the chip. It is recommended to add a shunt resistance of 1k-2k ohm between the VCC and AVDD. Refer to Chapter 7 for specific resistance calculations. There must be a decoupling capacitor higher than or equal to 100uF between the VCC pin and the ground.
12	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
13	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
14	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
15	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
16	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
17	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
18	GND	Ground
19	P1_1	P1.1
	OPA0_IP	OPA0 positive input
20	P1_2	P1.2
	OPA0_IN	OPA0 negative input
21	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
22	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
23	P1_4	P1.4

	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
24	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12
	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13

3.1.13 LKS32MC039DK6Q8B/ LKS32MC039DK6Q8C

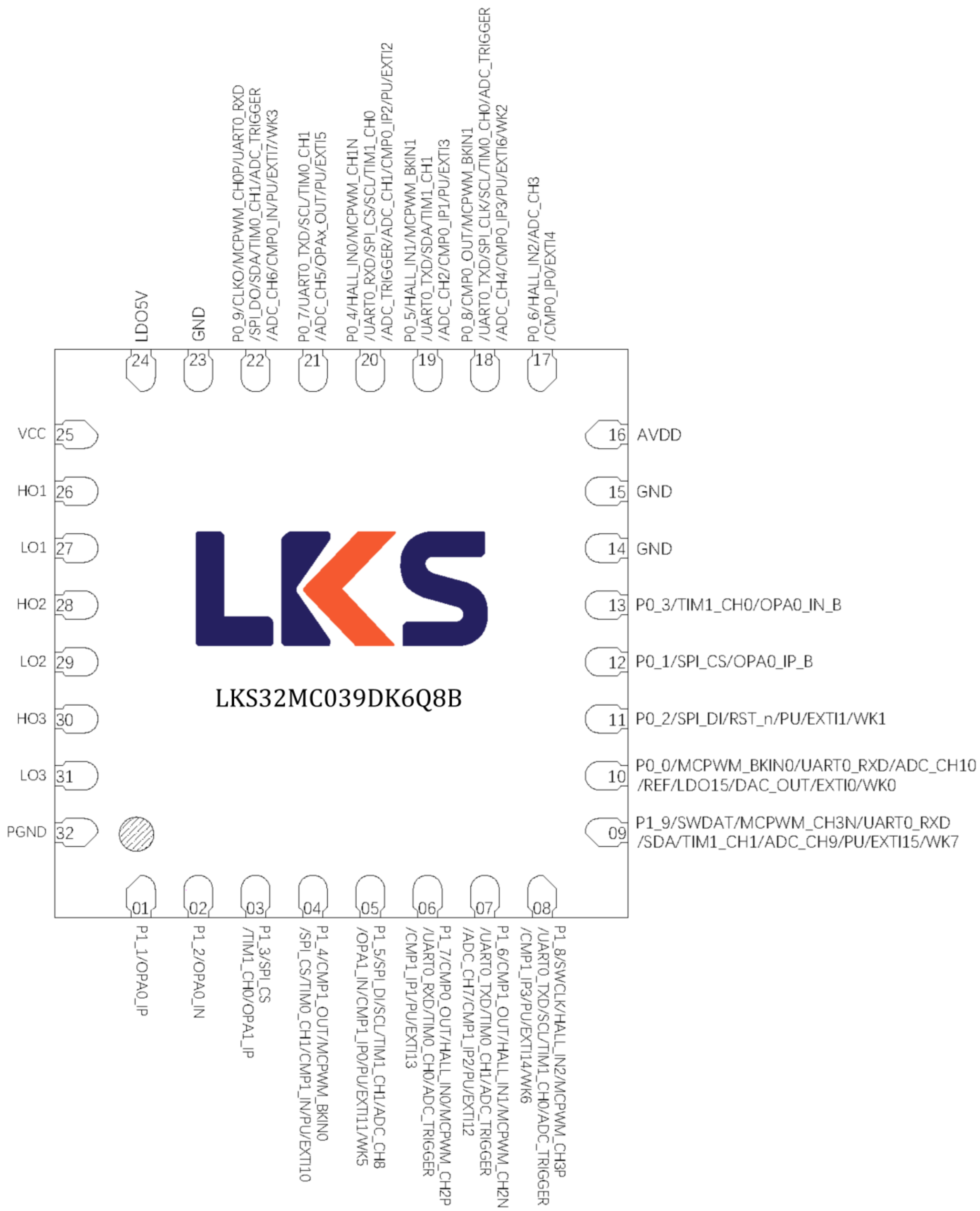

Figure 3-21 LKS32MC039DK6Q8B(C) Pin Assignment Diagram

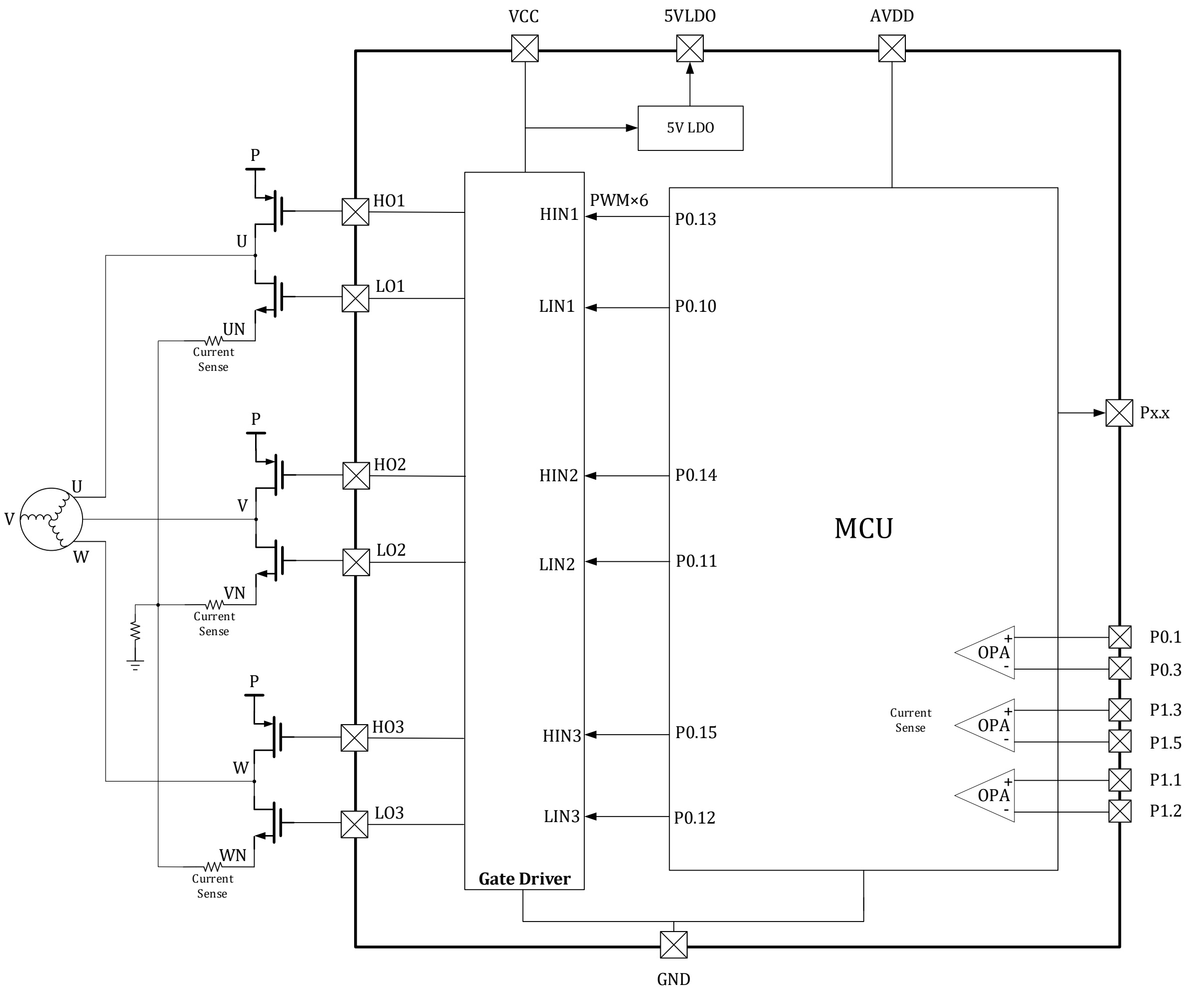

Figure 3-22 Schematic diagram of the LKS32MC039DK6Q8B(C) gate driver connection

Table 3-12 LKS32MC039DK6Q8B(C) Pin Description

0	GND	Ground in the belly of the chip
1	P1_1	P1.1
	OPA0_IP	OPA0 positive input
2	P1_2	P1.2
	OPA0_IN	OPA0 negative input
3	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
4	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software

	EXTI10	External GPIO interrupt input signal 10
5	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
6	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
7	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12
8	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6

9	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
10	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
11	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
12	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
13	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
14	GND	Ground
15	GND	Ground
16	AVDD	MCU low voltage power supply, should be 2.5-5.5V. In applications with good heat dissipation conditions, it can be directly connected to the 5V LDO pin of the chip. Connect this pin to an external 5V power supply if you are considering reducing the system power consumption using a 5V power supply generated by an external DCDC or charge pump.
17	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3

	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
18	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
19	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
20	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2
21	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output

	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
22	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
23	GND	Ground
24	LDO5V	5V LDO output. It is recommended to connect an external 1uF decoupling capacitor, as close as possible to the LDO5V pin.
25	VCC	This pin is power supply. If VCC is higher than 20V, the AVDD pin is powered by the LDO5V output of the chip. It is recommended to add a shunt resistance of 1k-2k ohm between the VCC and AVDD. Refer to Chapter 7 for specific resistance calculations. There must be a decoupling capacitor higher than or equal to 1uF between the VCC pin and the ground.
26	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
27	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
28	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
29	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
30	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
31	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
32	PGND	Power ground

3.1.14 LKS32MC039D2KQ8C

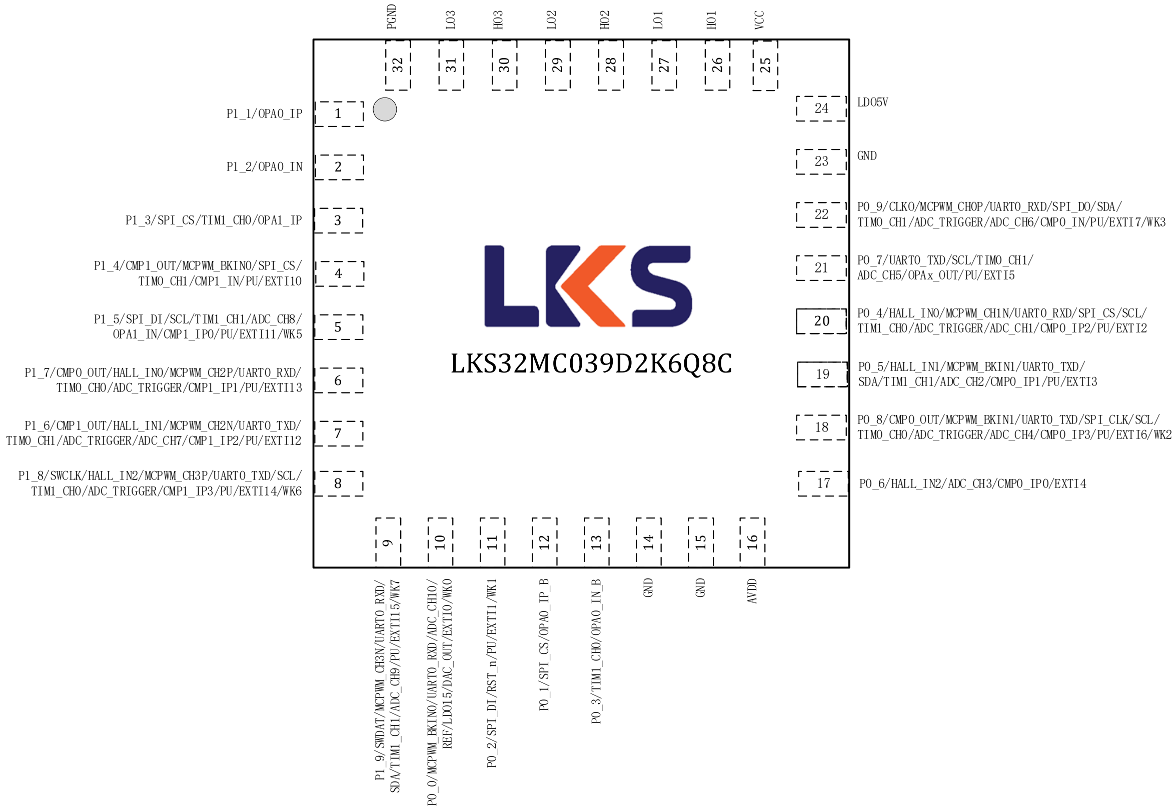

Figure 3-23 LKS32MC039D2K6Q8C Pin Assignment Diagram

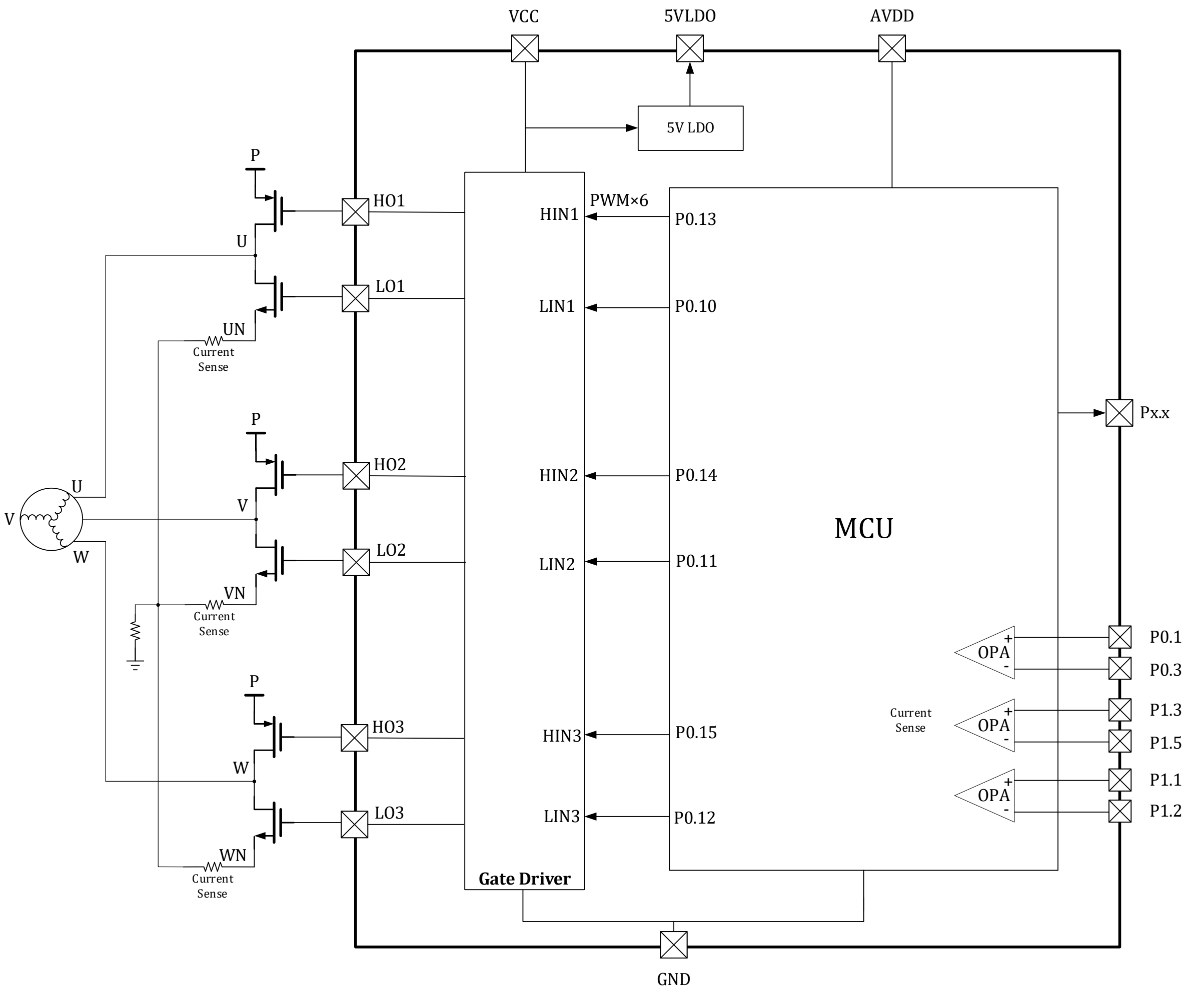

Figure 3-24 Schematic diagram of the LKS32MC039D2K6Q8C gate driver connection

Table 3-13 LKS32MC039D2K6Q8C Pin Description

0	GND	Ground in the belly of the chip
1	P1_1	P1.1
	OPA0_IP	OPA0 positive input
2	P1_2	P1.2
	OPA0_IN	OPA0 negative input
3	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
4	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software

	EXTI10	External GPIO interrupt input signal 10
5	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
6	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
7	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12
8	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6

9	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
10	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
11	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
12	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
13	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
14	GND	Ground
15	GND	Ground
16	AVDD	MCU low voltage power supply, should be 2.5-5.5V. In applications with good heat dissipation conditions, it can be directly connected to the 5V LDO pin of the chip. Connect this pin to an external 5V power supply if you are considering reducing the system power consumption using a 5V power supply generated by an external DCDC or charge pump.
17	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3

	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
18	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
19	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
20	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2
21	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output

	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
22	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
23	GND	Ground
24	LDO5V	5V LDO output. It is recommended to connect an external 1uF decoupling capacitor, as close as possible to the LDO5V pin.
25	VCC	This pin is power supply. If VCC is higher than 20V, the AVDD pin is powered by the LDO5V output of the chip. It is recommended to add a shunt resistance of 1k-2k ohm between the VCC and AVDD. Refer to Chapter 7 for specific resistance calculations. There must be a decoupling capacitor higher than or equal to 1uF between the VCC pin and the ground.
26	HO1	Phase A high-side output, worked by MCU P0.13; the polarity of HO1 is the same as that of P0.13, i.e. when P0.13 = 1, HO1 = 1. You need to set MCPWM_SWAP = 1.
27	LO1	Phase A low-side output, worked by MCU P0.10; the polarity of LO1 is the same as that of P0.10, i.e. when P0.10 = 1, LO1 = 1. You need to set MCPWM_SWAP = 1.
28	HO2	Phase B high-side output, worked by MCU P0.14; the polarity of HO2 is the same as that of P0.14, i.e. when P0.14 = 1, HO2 = 1. You need to set MCPWM_SWAP = 1.
29	LO2	Phase B low-side output, worked by MCU P0.11; the polarity of LO2 is the same as that of P0.11, i.e. when P0.11 = 1, LO2 = 1. You need to set MCPWM_SWAP = 1.
30	HO3	Phase C high-side output, worked by MCU P0.15; the polarity of HO3 is the same as that of P0.15, i.e. when P0.15 = 1, HO3 = 1. You need to set MCPWM_SWAP = 1.
31	LO3	Phase C low-side output, worked by MCU P0.12; the polarity of LO3 is the same as that of P0.12, i.e. when P0.12 = 1, LO3 = 1. You need to set MCPWM_SWAP = 1.
32	PGND	Power ground

3.1.15 LKS32MC039PL5K6Q8B/ LKS32MC039PL5K6Q8C

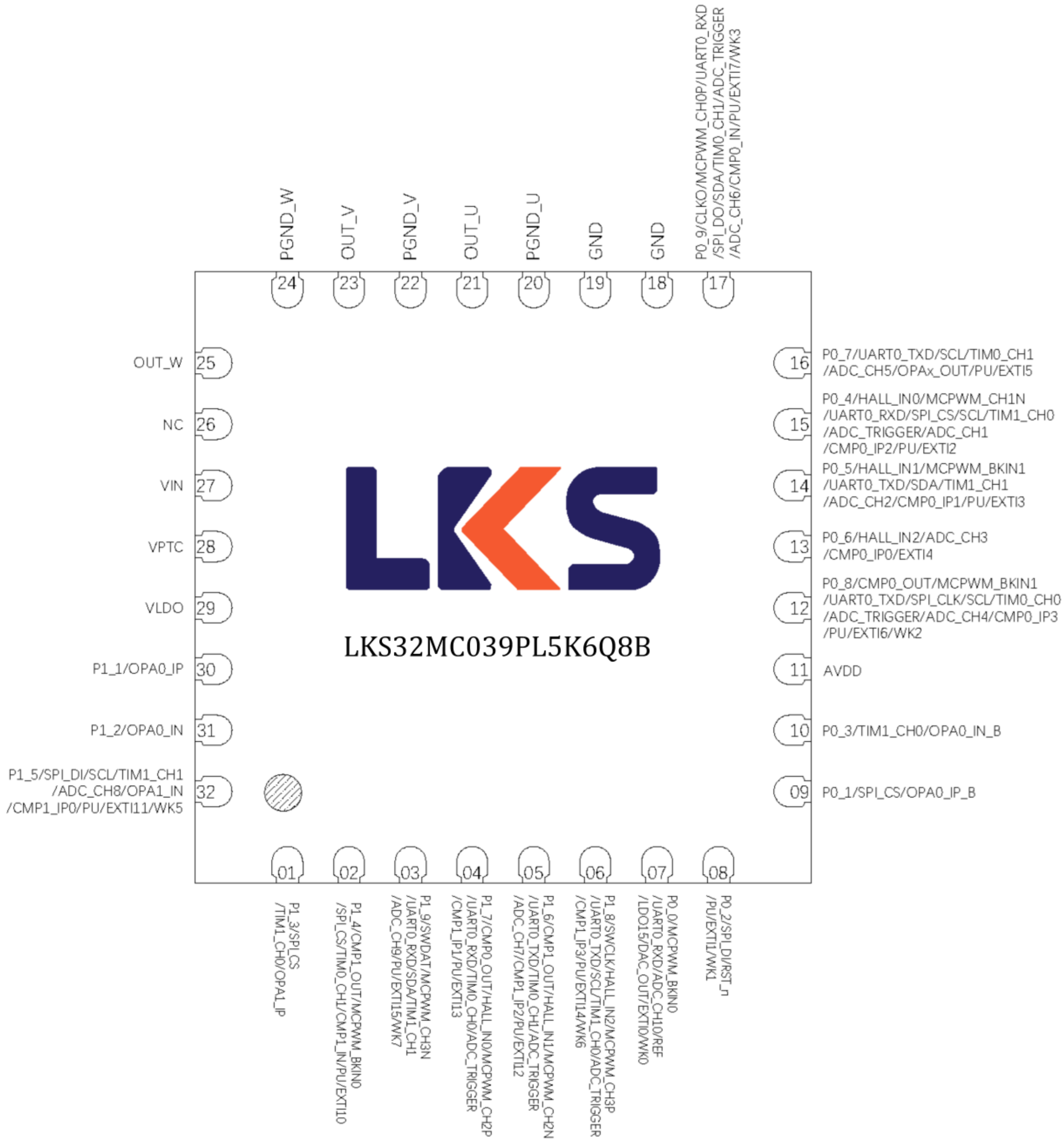

Figure 3-25 LKS32MC039PL5K6Q8B(C) Pin Assignment Diagram

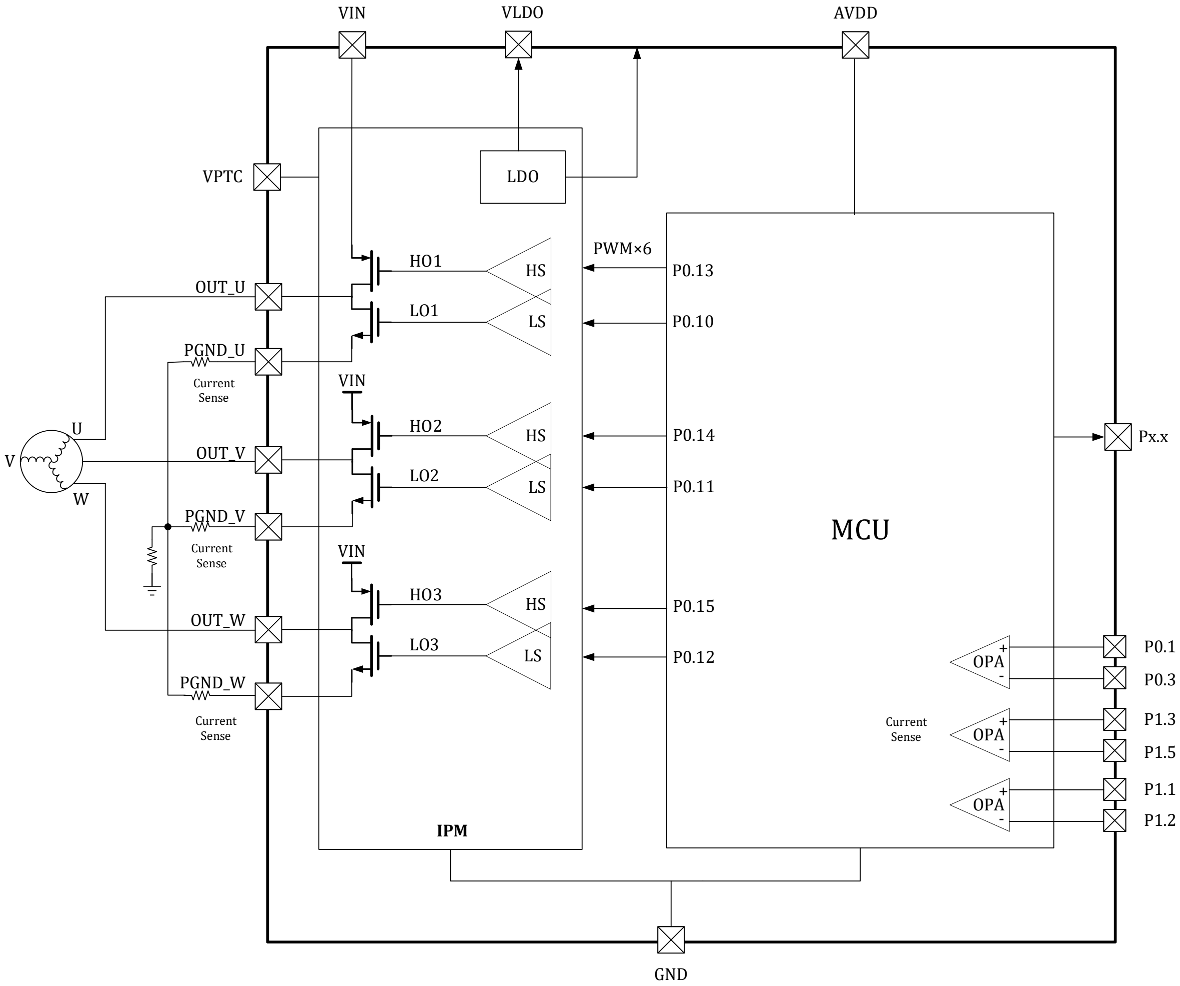

Figure 3-26 Schematic diagram of the LKS32MC039PL5K6Q8B(C) gate driver connection

Table 3-14 LKS32MC039PL5K6Q8B(C) Pin Description

0	GND	Ground in the belly of the chip
1	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
2	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
3	P1_9	P1.9
	SWDAT	SWD Data

	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
4	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
5	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 12
6	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
7	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0

	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
8	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
9	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
10	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
11	AVDD	MCU low voltage power supply, should be 2.5-5.5V. In applications with good heat dissipation conditions, it can be directly connected to the 5V LDO pin of the chip. Connect this pin to an external 5V power supply if you are considering reducing the system power consumption using a 5V power supply generated by an external DCDC or charge pump.
12	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
13	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0

	EXTI4	External GPIO interrupt input signal 4
14	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI3	External GPIO interrupt input signal 3
15	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2
16	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
17	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7

	WK3	External wake-up signal 3
18	GND	Ground
19	GND	Ground
20	PGND_U	U phase power ground
21	OUT_U	U phase output, Controlled by P0.15 (P) and P0.14 (N). The truth table is available in the MOS section.
22	PGND_V	V phase power ground
23	OUT_V	V phase output, Controlled by P0.13 (P) and P0.12 (N). The truth table is available in the MOS section.
24	PGND_W	W phase power ground
25	OUT_W	W phase output, Controlled by P0.11 (P) and P0.10 (N). The truth table is available in the MOS section.
26	NC	
27	VIN	This pin is a chip supply.
28	VPTC	Temperature detection pin
29	VLDO	5V LDO output. It is recommended to connect an external 1uF decoupling capacitor, as close as possible to the LDO5V pin.
30	P1_1	P1.1
	OPA0_IP	OPA0 positive input
31	P1_2	P1.2
	OPA0_IN	OPA0 negative input
32	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5

3.1.16 LKS32MC039PL3K6Q8B/ LKS32MC039PL3K6Q8C

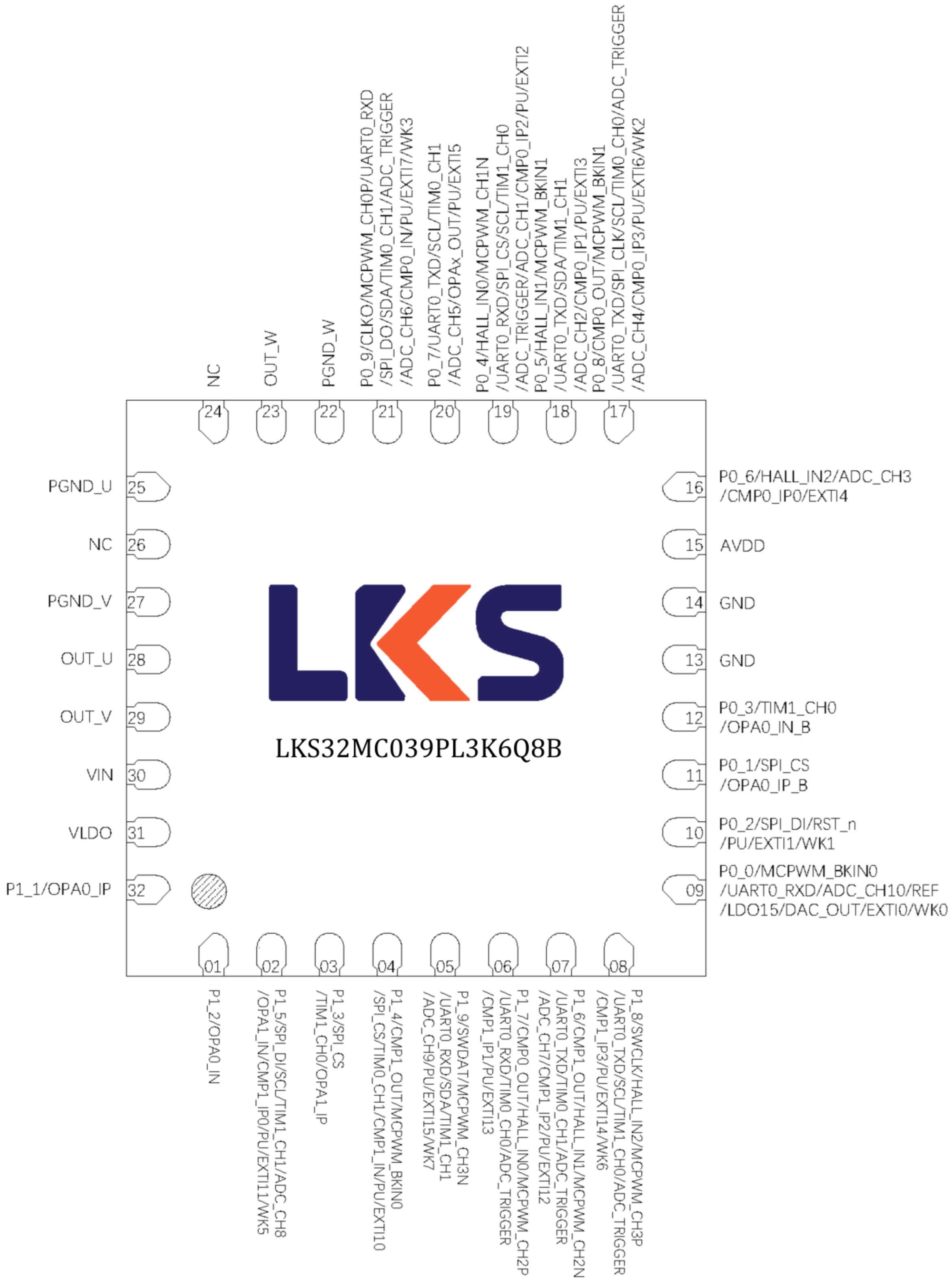

Figure 3-27 LKS32MC039PL3K6Q8B(C) Pin Assignment Diagram

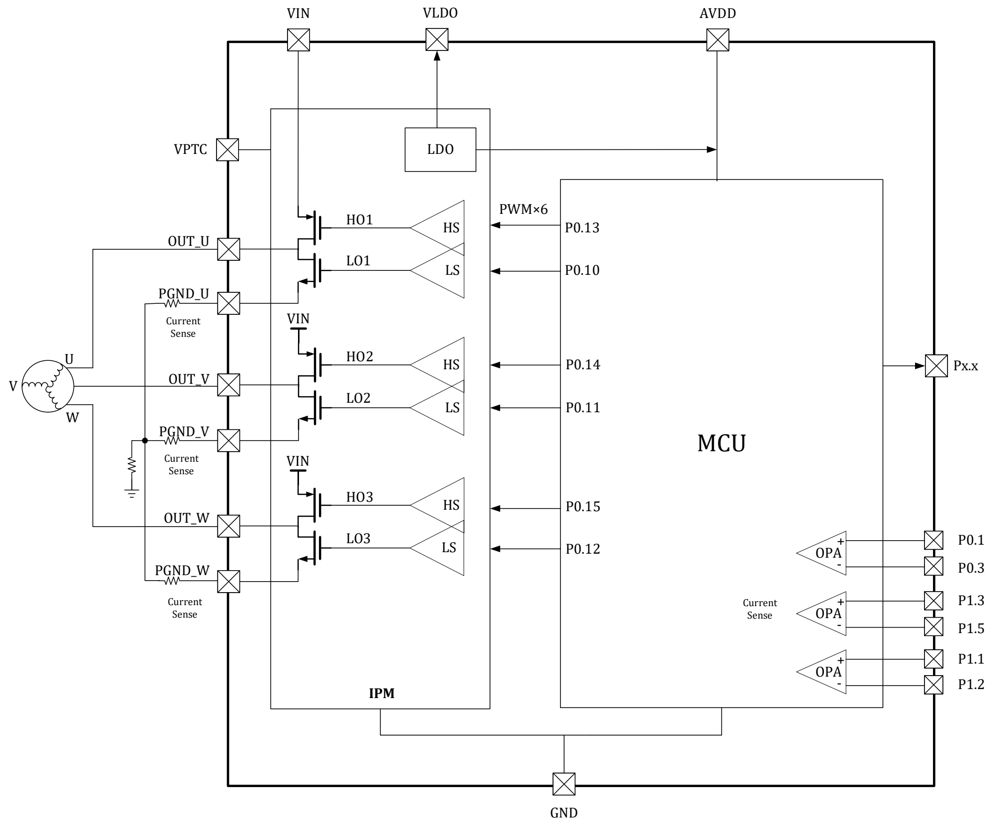

Figure 3-28 Schematic diagram of the LKS32MC039PL3K6Q8B gate driver connection

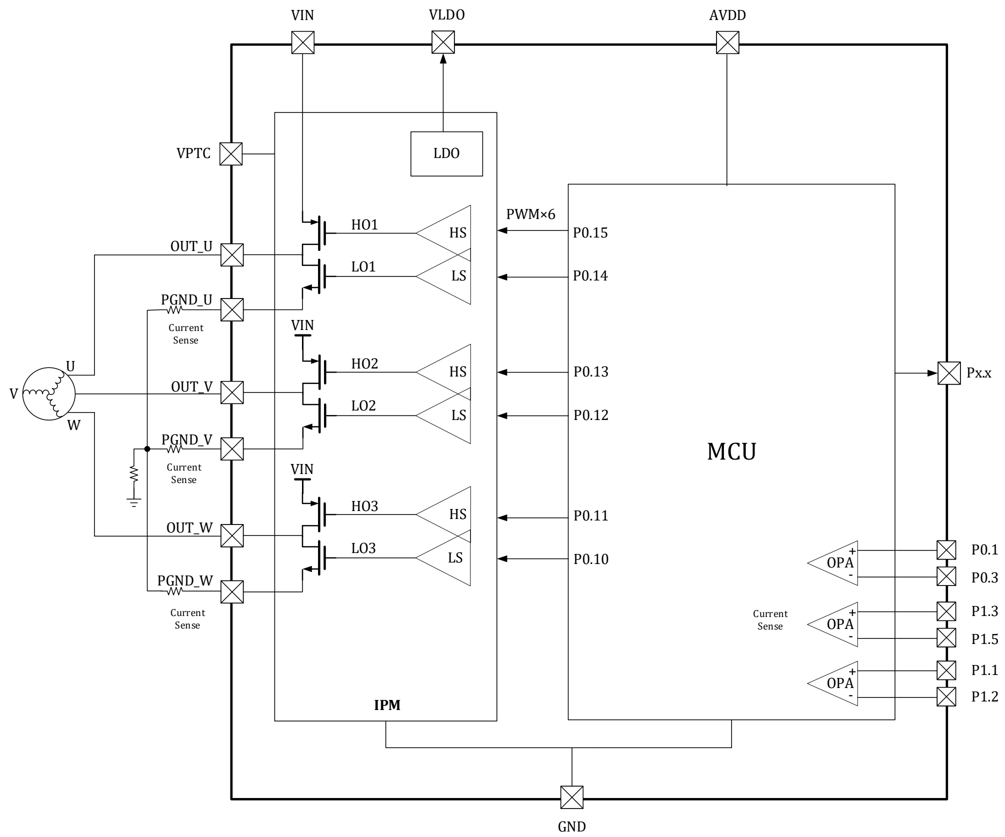

Figure 3-29 Schematic diagram of the LKS32MC039PL3K6Q8C gate driver connection

Table 3-15 LKS32MC039PL3K6Q8B(C) Pin Description

0	GND	Ground in the belly of the chip
1	P1_2	P1.2
	OPA0_IN	OPA0 negative input
2	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO interrupt input signal 11
	WK5	External wake-up signal 5
3	P1_3	P1.3
	SPI_CS	SPI chip select
	TIM1_CH0	Timer1 channel0
	OPA1_IP	OPA1 positive input
4	P1_4	P1.4
	CMP1_OUT	Comparator 1 output
	MCPWM_BKIN0	PWM break signal 0
	SPI_CS	SPI chip select
	TIM0_CH1	Timer0 channel1
	CMP1_IN	Comparator1 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI10	External GPIO interrupt input signal 10
5	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO interrupt input signal 15
	WK7	External wake-up signal 7
6	P1_7	P1.7
	CMP0_OUT	Comparator 0 output
	HALL_IN0	Hall interface input 0
	MCPWM_CH2P	PWM channel 2 high-side
	UART0_RXD	UART0 receive(transmit)

	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP1	Comparator1 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI13	External GPIO interrupt input signal 13
7	P1_6	P1.6
	CMP1_OUT	Comparator 1 output
	HALL_IN1	Hall interface input 1
	MCPWM_CH2N	PWM channel 2 low-side
	UART0_TXD	UART0 transmit(receive)
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH7	ADC channel 7
	CMP1_IP2	Comparator1 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI12	External GPIO interrupt input signal 12
8	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2
	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO interrupt input signal 14
	WK6	External wake-up signal 6
9	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO interrupt input signal 0
	WK0	External wake-up signal 0
10	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.

	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO interrupt input signal 1
	WK1	External wake-up signal 1
11	P0_1	P0.1
	SPI_CS	SPI chip select
	OPA0_IP_B	OPA0 positive input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
12	P0_3	P0.3
	TIM1_CH0	Timer1 channel0
	OPA0_IN_B	OPA0 negative input B, if input B is used, you should set SYS_AFE_REG0[5] = 1
13	GND	Ground
14	GND	Ground
15	AVDD	MCU low voltage power supply, should be 2.5-3.6V. In applications with good heat dissipation conditions, it can be directly connected to the 3.3V LDO pin of the chip. Connect this pin to an external 3.3V power supply if you are considering reducing the system power consumption using a 3.3V power supply generated by an external DCDC or charge pump.
16	P0_6	P0.6
	HALL_IN2	Hall interface input 2
	ADC_CH3	ADC channel 3
	CMP0_IP0	Comparator0 positive input0
	EXTI4	External GPIO interrupt input signal 4
17	P0_8	P0.8
	CMP0_OUT	Comparator 0 output
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH0	Timer0 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH4	ADC channel 4
	CMP0_IP3	Comparator0 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI6	External GPIO interrupt input signal 6
	WK2	External wake-up signal 2
18	P0_5	P0.5
	HALL_IN1	Hall interface input 1
	MCPWM_BKIN1	PWM break signal 1
	UART0_TXD	UART0 transmit(receive)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH2	ADC channel 2
	CMP0_IP1	Comparator0 positive input1
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software

	EXTI3	External GPIO interrupt input signal 3
19	P0_4	P0.4
	HALL_IN0	Hall interface input 0
	MCPWM_CH1N	PWM channel 1 low-side
	UART0_RXD	UART0 receive(transmit)
	SPI_CS	SPI chip select
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH1	ADC channel 1
	CMP0_IP2	Comparator0 positive input2
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI2	External GPIO interrupt input signal 2
20	P0_7	P0.7
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM0_CH1	Timer0 channel1
	ADC_CH5	ADC channel 5
	OPAx_OUT	OPA output
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI5	External GPIO interrupt input signal 5
21	P0_9	P0.9
	CLKO	Clock output for debug
	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO interrupt input signal 7
	WK3	External wake-up signal 3
22	PGND_W	W phase power ground
23	OUT_W	W phase output, Controlled by P0.15 (P) and P0.12 (N). The truth table is available in the MOS section.
24	NC	
25	PGND_U	U phase power ground
26	NC	
27	PGND_V	V phase power ground
28	OUT_U	U phase output, Controlled by P0.13 (P) and P0.10 (N). The truth table is available in the MOS section.

29	OUT_V	V phase output, Controlled by P0.14 (P) and P0.11 (N). The truth table is available in the MOS section.
30	VIN	This pin is a chip supply.
31	VLDO	3.3V LDO output. It is recommended to connect an external 1uF decoupling capacitor, as close as possible to the LDO5V pin.
32	P1_1	P1.1
	OPA0_IP	OPA0 positive input

3.2 Pin Multiplexing

Table 3-16 LKS32MC03x Pin Function Selection

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0
P0.0			MCPWM_BKIN0	UART0_R(T)XD						ADC_CH10/REF/LDO15/DAC_OUT
P0.1					SPI_CS					OPA0_IP_B
P0.2					SPI_DI(O)					RST_n
P0.3								TIM1_CH0		OPA0_IN_B
P0.4		HALL_IN0	MCPWM_CH1N	UART0_R(T)XD	SPI_CS	SCL		TIM1_CH0	ADC_TRIGGER	ADC_CH1/CMP0_IP2
P0.5		HALL_IN1	MCPWM_BKIN1	UART0_T(R)XD		SDA		TIM1_CH1		ADC_CH2/CMP0_IP1
P0.6		HALL_IN2								ADC_CH3/CMP0_IP0
P0.7				UART0_T(R)XD		SCL	TIM0_CH1			ADC_CH5/OPAx_OUT
P0.8	CMP0_OUT		MCPWM_BKIN1	UART0_T(R)XD	SPI_CLK	SCL	TIM0_CH0		ADC_TRIGGER	ADC_CH4/CMP0_IP3
P0.9	CLKO		MCPWM_CH0P	UART0_R(T)XD	SPI_DO(I)	SDA	TIM0_CH1		ADC_TRIGGER	CMP0_IN
P0.10	CLKO		MCPWM_CH0P				TIM0_CH0	TIM1_CH0		ADC_CH6
P0.11			MCPWM_CH0N		SPI_CLK			TIM1_CH1		
P0.12			MCPWM_CH1P		SPI_DO(I)		TIM0_CH1			
P0.13			MCPWM_CH1N		SPI_DI(O)			TIM1_CH1		
P0.14			MCPWM_CH2P				TIM0_CH0			
P0.15			MCPWM_CH2N					TIM1_CH0		ADC_CH7

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0
P1.1										OPA0_IP
P1.2										OPA0_IN
P1.3					SPI_CS			TIM1_CH0		OPA1_IP
P1.4	CMP1_OUT		MCPWM_BKIN0		SPI_CS		TIM0_CH1			CMP1_IN
P1.5					SPI_DI(O)	SCL		TIM1_CH1		OPA1_IN/CMP1_IP0
P1.6	CMP1_OUT	HALL_IN1	MCPWM_CH2N	UART0_T(R)XD			TIM0_CH1		ADC_TRIGGER	CMP1_IP2
P1.7	CMP0_OUT	HALL_IN0	MCPWM_CH2P	UART0_R(T)XD			TIM0_CH0		ADC_TRIGGER	CMP1_IP1
P1.8	SWCLK	HALL_IN2	MCPWM_CH3P	UART0_T(R)XD		SCL		TIM1_CH0	ADC_TRIGGER	CMP1_IP3
P1.9	SWDAT		MCPWM_CH3N	UART0_R(T)XD		SDA		TIM1_CH1		ADC_CH9

Table 3-17 LKS32MC03xB Pin Function Selection

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0
P0.0			MCPWM_BKIN0	UART0_R(T)XD						ADC_CH10/REF/LDO15/DAC_OUT
P0.1					SPI_CS					OPA0_IP_B
P0.2					SPI_DI(O)					RST_n
P0.3								TIM1_CH0		OPA0_IN_B
P0.4		HALL_IN0	MCPWM_CH1N	UART0_R(T)XD	SPI_CS	SCL		TIM1_CH0	ADC_TRIGGER	ADC_CH1/CMP0_IP2
P0.5		HALL_IN1	MCPWM_BKIN1	UART0_T(R)XD				TIM1_CH1		ADC_CH2/CMP0_IP1
P0.6		HALL_IN2								ADC_CH3/CMP0_IP0
P0.7				UART0_T(R)XD		SCL	TIM0_CH1			ADC_CH5/OPAx_OUT
P0.8	CMP0_OUT		MCPWM_BKIN1	UART0_T(R)XD	SPI_CLK	SCL	TIM0_CH0		ADC_TRIGGER	ADC_CH4/CMP0_IP3
P0.9	CLKO		MCPWM_CH0P	UART0_R(T)XD	SPI_DO(I)	SDA	TIM0_CH1		ADC_TRIGGER	ADC_CH6/CMP0_IN
P0.10	CLKO		MCPWM_CH0P				TIM0_CH0	TIM1_CH0		
P0.11			MCPWM_CH0N		SPI_CLK			TIM1_CH1		
P0.12			MCPWM_CH1P		SPI_DO(I)		TIM0_CH1			
P0.13			MCPWM_CH1N		SPI_DI(O)			TIM1_CH1		
P0.14			MCPWM_CH2P				TIM0_CH0			
P0.15			MCPWM_CH2N					TIM1_CH0		

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0
P1.1										OPA0_IP
P1.2										OPA0_IN
P1.3					SPI_CS			TIM1_CH0		OPA1_IP
P1.4	CMP1_OUT		MCPWM_BKIN0		SPI_CS		TIM0_CH1			CMP1_IN
P1.5					SPI_DI(O)	SCL		TIM1_CH1		ADC_CH8/OPA1_IN/CMP1_IP0
P1.6	CMP1_OUT	HALL_IN1	MCPWM_CH2N	UART0_T(R)XD			TIM0_CH1		ADC_TRIGGER	ADC_CH7/CMP1_IP2
P1.7	CMP0_OUT	HALL_IN0	MCPWM_CH2P	UART0_R(T)XD			TIM0_CH0		ADC_TRIGGER	CMP1_IP1
P1.8	SWCLK	HALL_IN2	MCPWM_CH3P	UART0_T(R)XD		SCL		TIM1_CH0	ADC_TRIGGER	CMP1_IP3
P1.9	SWDAT		MCPWM_CH3N	UART0_R(T)XD		SDA		TIM1_CH1		ADC_CH9

4 Package Dimensions

4.1 LKS32MC031PC6Q8C

DFN5.0*6.0_48L

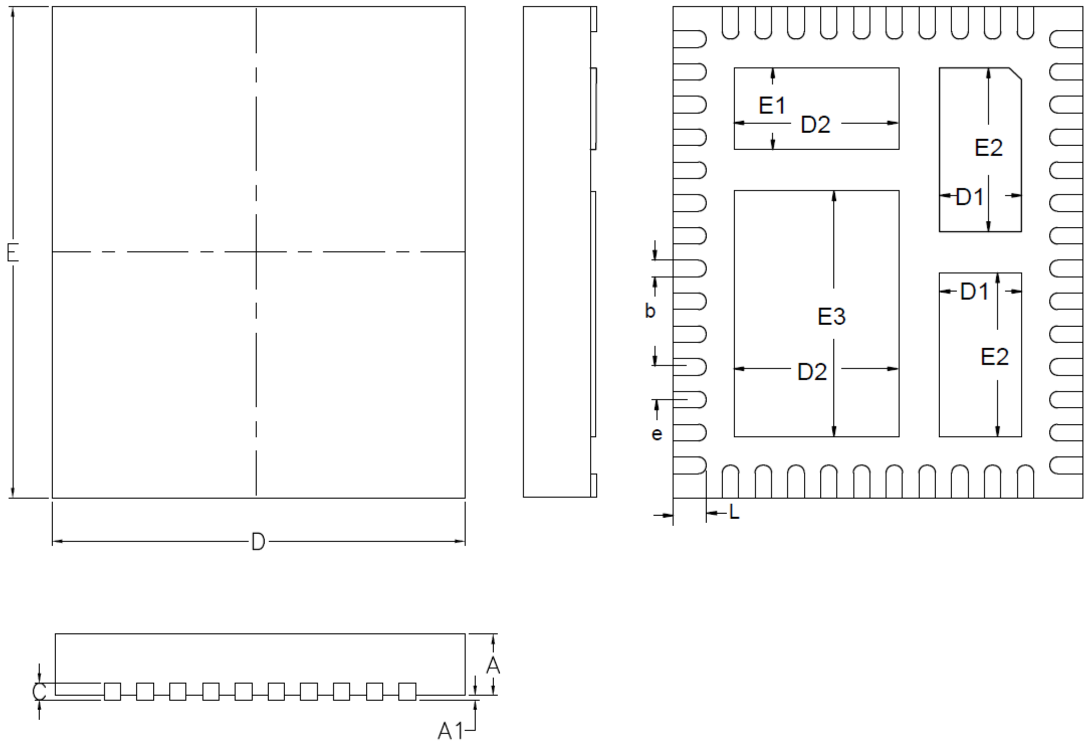

Figure 4- 1 LKS32MC031PC6Q8C Packaging

Table 4- 1 LKS32MC031PC6Q8C Package Dimensions

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.15	0.20	0.25
D	4.90	5.00	5.10
D1	0.90	1.00	1.10
D2	1.90	2.00	2.10
e		0.40	
E	5.90	6.00	6.10
E1	0.90	1.00	1.10
E2	1.90	2.00	2.10
E3	2.90	3.00	3.10
L	0.30	0.40	0.50

4.2 LKS32MC033PH6Q8C

QFN20 3*3

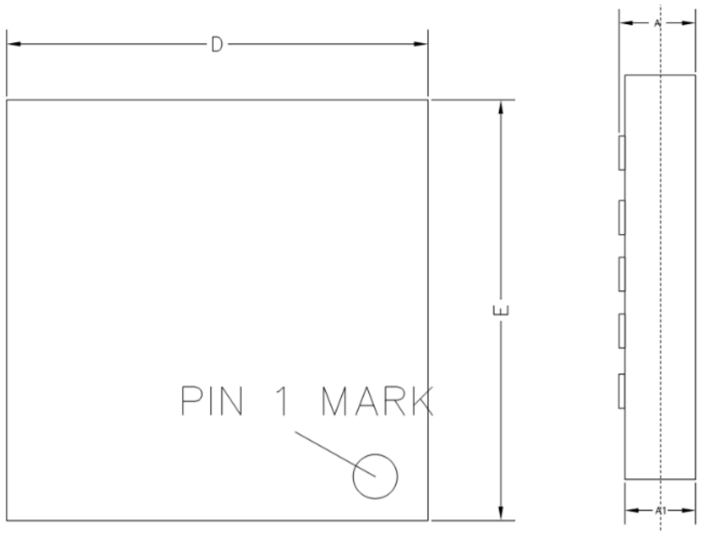

Figure 4- 2 LKS32MC033PH6Q8C Packaging

Table 4- 2 LKS32MC033PH6Q8C Package Dimensions

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.007	0.012	0.017
D	2.900	3.000	3.100
E	2.900	3.000	3.100
D1	1.150	1.200	1.250
E1	0.950	1.000	1.050
L	0.350	0.400	0.450
b	0.150	0.200	0.250
e	0.350	0.400	0.450
e1	0.350	0.400	0.450
e2	0.550	0.600	0.650
X1	0.550	0.600	0.650
X2	0.550	0.600	0.650

4.3 LKS32MC035DL6S8(B/C)/ LKS32MC035EL6S8B(C)

SOP16L:

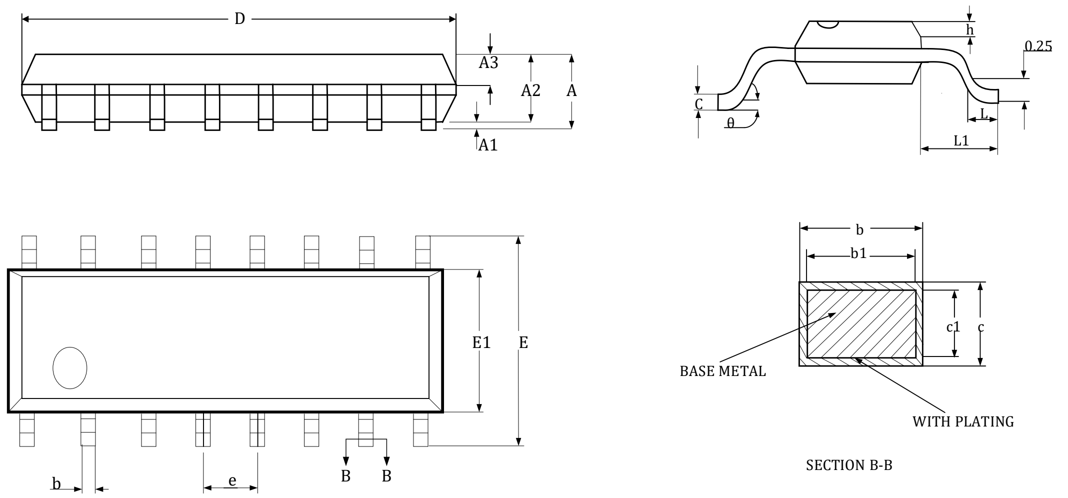

Figure 4- 3 LKS32MC035DL6S8(B/C)/ LKS32MC035EL6S8B(C) Packaging

Table 4- 3 LKS32MC035DL6S8(B/C)/ LKS32MC035EL6S8B(C) Package Dimensions

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
b1	0.38	0.41	0.44
c	0.20	-	0.25
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.15	2.25	2.35
e	1.27 BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

4.4 LKS32MC037EM6S8(B/C)/LKS32MC037FM6S8B(C)

SSOP24L:

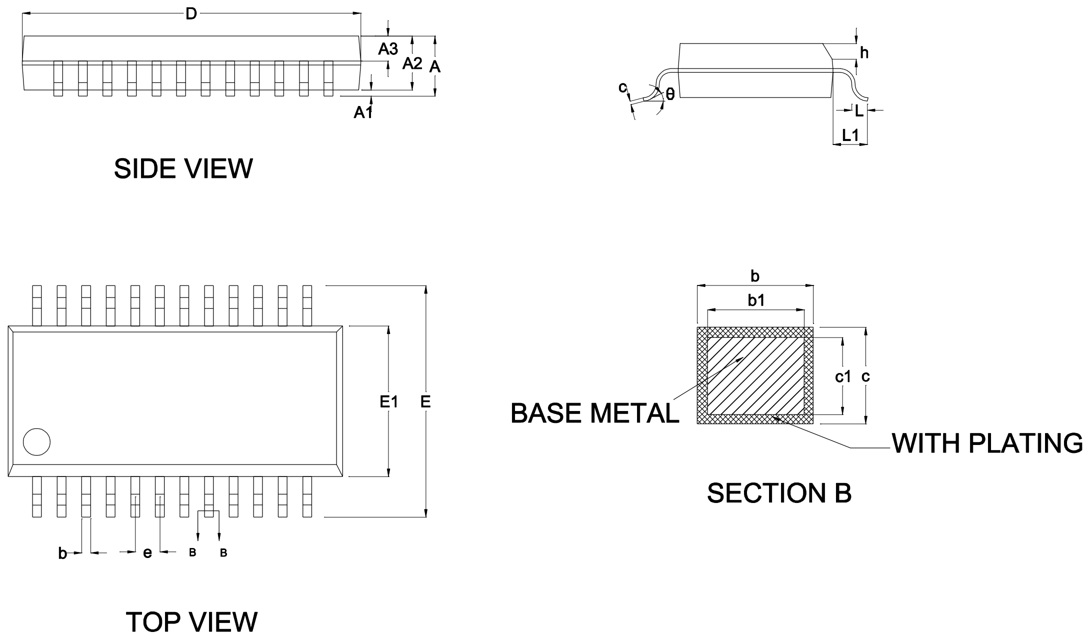

Figure 4- 4 LKS32MC037(E/F)M6S8(B/C) Packaging

Table 4- 4 LKS32MC037(E/F)M6S8(B/C) Package Dimensions

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

4.5 LKS32MC037Q(2)M6Q8(B/C)

QFN4*4 24L-0.75:

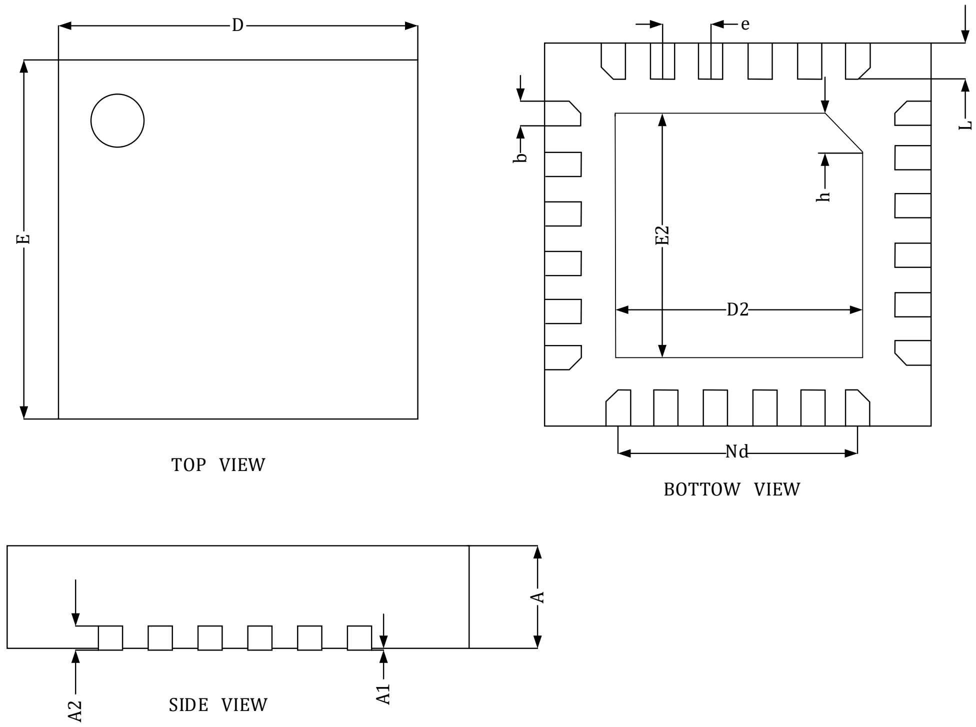

Figure 4- 5 LKS32MC037Q(2)M6Q8(B/C) Packaging

Table 4- 5 LKS32MC037Q(2)M6Q8(B/C) Package Dimensions

SYMBOL	MLLMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.203 REF		
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
Nd	2.50 BSC		
e	0.50 BSC		
L	0.35	0.40	0.45
b	0.20	0.25	0.30
h	0.30	0.35	0.40

4.6 LKS32MC039DK6Q8B(C)/LKS32MC039PL3K6Q8B(C)

QFN4*4 32L-0.75 Profile Quad Flat Package:

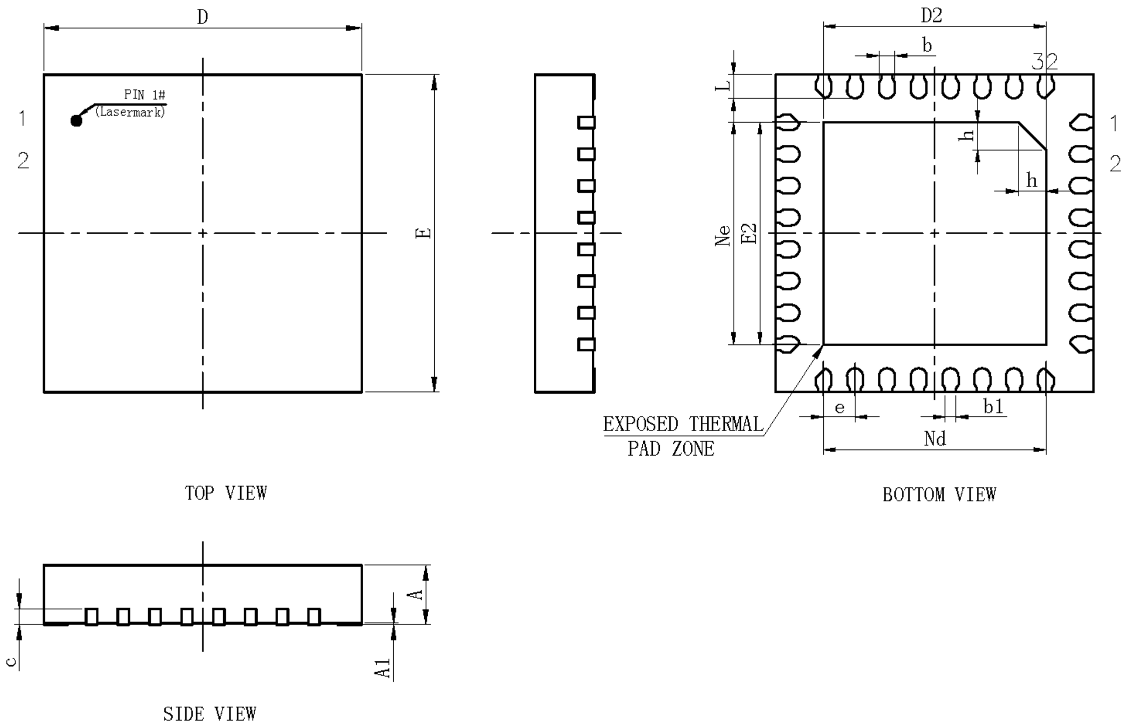

Figure 4- 6 LKS32MC039DK6Q8B(C)/LKS32MC039PL3K6Q8B(C) Packaging

Table 4- 6 LKS32MC039DK6Q8B(C)/LKS32MC039PL3K6Q8B(C) Package Dimensions

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	0	0. 02	0. 05
b	0. 15	0.20	0. 25
b1	0.14REF		
c	0.18	0.20	0.25
D	3. 90	4. 00	4. 10
D2	2. 60	2. 65	2. 70
e	0. 40BSC		
Nd	2. 80BSC		
E	3. 90	4. 00	4. 10
E2	2. 60	2. 65	2. 70
Ne	2. 80BSC		
K	0. 20	–	–
L	0. 35	0. 40	0. 45
L1	0. 30	0. 35	0. 40
L2	0. 15	0. 20	0. 25
h	0. 30	0. 35	0. 40

4.7 LKS32MC039PL3K6Q8C

QFN4*4 32L-0.55 Profile Quad Flat Package:

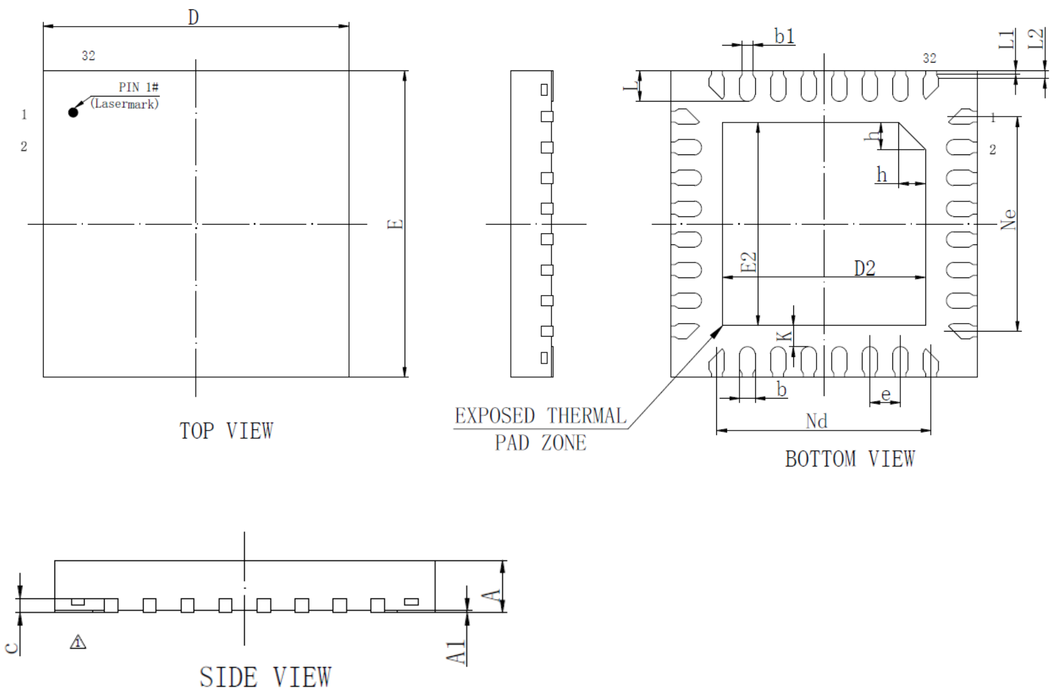

Figure 4- 7 LKS32MC039PL3K6Q8C Packaging

Table 4- 7 LKS32MC039PL3K6Q8C Package Dimensions

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 50	0.55	0. 60
A1	0	0. 02	0. 05
b	0. 15	0.20	0. 25
b1	0.14REF		
c	0.10	0.15	0.20
D	3. 90	4. 00	4. 10
D2	2. 55	2. 65	2. 75
e	0. 40BSC		
Nd	2. 80BSC		
E	3. 90	4. 00	4. 10
E2	2. 55	2. 65	2. 75
Ne	2. 80BSC		
L	0. 35	0. 40	0. 45
L1	0	0. 05	0. 10
L2	0. 05	0. 10	0. 15
h	0. 30	0. 35	0. 40
K	0. 20	–	–

4.8 LKS32MC039PL5K6Q8B(C)

QFN5*5 32L-0.75 Profile Quad Flat Package:

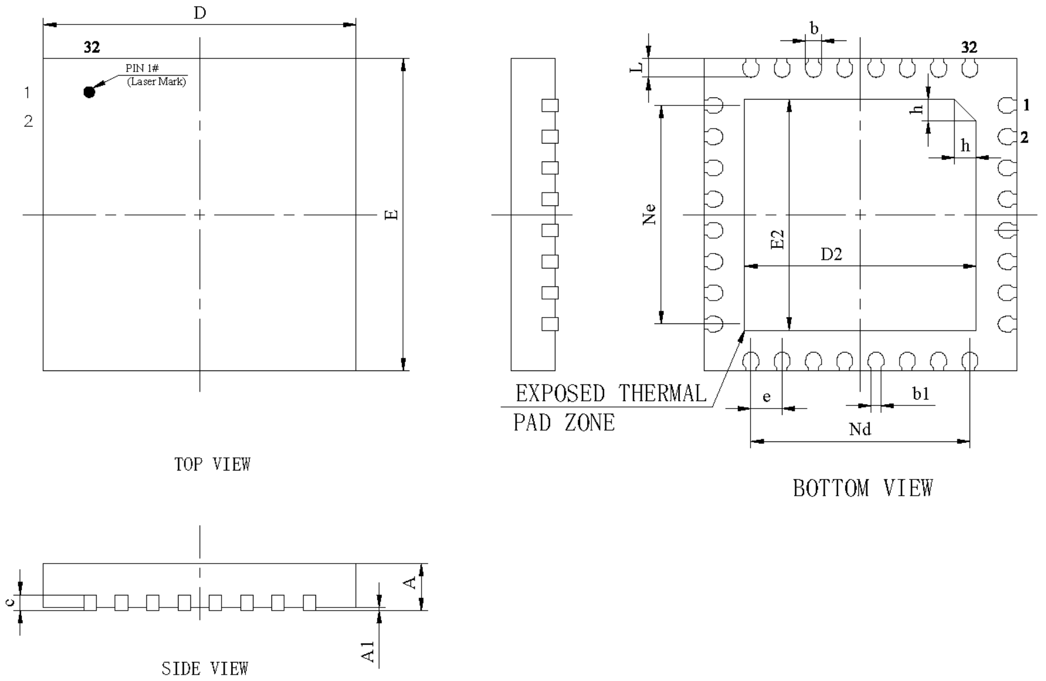

Figure 4- 8 LKS32MC039PL5K6Q8B(C) Packaging

Table 4- 8 LKS32MC039PL5K6Q8B(C) Package Dimensions

SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0. 70	0.75	0. 80	
	0. 80	0.85	0. 90	⚠1
	0. 85	0.90	0. 95	⚠2
A1	0.00	0.02	0. 05	
b	0. 20	0.25	0. 30	
b1	0.16REF			
c	0. 18	0.20	0. 25	
D	4. 90	5. 00	5. 10	
D2	3. 70	3. 80	3. 90	
e	0. 50BSC			
Ne	3. 50BSC			
Nd	3. 50BSC			
E	4. 90	5. 00	5. 10	
E2	3. 70	3. 80	3. 90	
L	0. 25	0.30	0. 35	
h	0. 30	0. 35	0. 40	
L/F载体尺寸	4. 10X4. 10			

5 Electrical Characteristics

Table 5-1 LKS32MC03x Electrical Limit Parameter

Parameter	Min.	Max.	Unit	Description
MCU Supply Voltage (AVDD)	-0.3	+6.0	V	
Gate Driver Supply Voltage (VCC)	-0.3	+40.0	V	LKS03x with 3P3N driver
5V LDO output current		40	mA	035DL6S8(B/C)/037EM6S8(B/C)/037QM6Q8(B/C)/039DK6Q8B(C)/LKS32MC039D2K6Q8C
		15	mA	035EL6S8(B/C)/037FM6S8(B/C)/031PC6Q8C (LDO maximum load 30mA, 5V case maximum load 15mA)
Operating temperature	-40	+105	˚C	
Storage temperature	-40	+150	˚C	
Junction temperature	-	125	°C	
Pin temperature	-	260	°C	Soldering for 10 sec

Table 5-2 LKS32MC03x Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Description
MCU Supply Voltage (AVDD)	2.5	5	5.5	V	
Analog Operating Voltage (AVDD$_A$)	2.8	5	5.5	V	REF2VDD=0, ADC uses internal 2.4V reference
	2.4	5	5.5	V	REF2VDD=1, ADC uses AVDD as reference
Gate Driver Supply Voltage(VCC)	7.5		32	V	035DL6S8(B/C)/ 037EM6S8(B/C)/ 037QM6Q8(B/C)/ 039DK6Q8B(C)/ LKS32MC039D2K6Q8C
	5.7		28		035EL6S8B(C)/ 037FM6S8B(C)/ 031PC6Q8C
LDO Supply Voltage(VCCLDO)	5.7		32	V	
MOS Supply Voltage(P)	3.3	24	40	V	LKS32MC039PL5K6Q8B
	3	9	12	V	LKS32MC039PL3K6Q8B
			30	V	LKS32MC031PC6Q8C

OPA could work under 2.5V, but the output range will be limited.

Table 5-3 LKS32MC03x ESD parameters

Item			Min.	Max.	Unit
ESD test (HBM)	LKS32MC035DL6S8(B/C) LKS32MC037EM6S8(B/C) LKS32MC037QM6Q8(B/C)	MCU	-6000	6000	V
		Gate driver	-2000	2000	V

	LKS32MC039DK6Q8(B/C) LKS32MC039D2K6Q8C				
	LKS32MC035EL6S8(B/C) LKS32MC037FM6S8(B/C) LKS32MC031PC6Q8C	MCU	-6000	6000	V
		Gate driver	-2000	2000	V

According to "MIL-STD-883J Method 3015.9", under the environment of 25°C and 55% relative humidity, electrostatic discharge is applied to all IO pins of the tested chip for 3 times, with an interval of 1s each time.

Table 5-4 LKS32MC03x Latch-up parameters

Item	Min.	Max.	Unit
Latch-up current (85°C)	-200	200	mA

According to "JEDEC STANDARD NO.78E NOVEMBER 2016", apply an overvoltage of 8V to all power IOs and inject 200mA of current on each signal IO.

Table 5-5 LKS32MC03x IO Limit Parameter

Parameter	Description	Minimum	Maximum	Unit
V_{IN}	Input voltage range for GPIO signals	-0.3	6.0	V
I_{INJ_PAD}	Maximum injection current for single GPIOs	-11.2	11.2	mA
I_{INJ_SUM}	Maximum injection current for all GPIOs	-50	50	mA

Table 5-6 LKS32MC03x IO DC Parameter

Parameter	Description	AVDD	Conditions	Min.	Max.	Unit
V_{IH}	High input level of digital IO	5V	-	3.04		V
		3.3V		2.05		
V_{IL}	Low input level of digital IO	5V	-		0.3*AVDD	V
		3.3V			0.8	
V_{HYS}	Schmidt hysteresis range	5V	-	0.1*AVDD		V
		3.3V				
I_{IH}	Digital IO current consumption when input is high	5V	-		1	uA
		3.3V				
I_{IL}	Digital IO current consumption when input is low	5V	-	-1		uA
		3.3V				
V_{OH}	High output level of digital IO		Current = 11.2mA	AVDD-0.8		V
V_{OL}	Low output level of digital IO		Current = 11.2mA		0.5	V
R_{pup}	Pull-up resistor*			8	12	kΩ
$R_{io\text{-}ana}$	Connection resistance between IO and internal analog circuit			100	200	Ω
C_{IN}	Digital IO Input-capacitance	5V	-		10	pF

		3.3V				

* Only part of IOs have built-in pull-up resistors. Please refer to the pin description section for details

Table 5-7 LKS32MC03x Current Consumption IDDQ

Clock	Operating mode	3.3V	5V	Unit
48MHz	CPU, flash, SRAM, MCPWM, Timer, and all analog modules are active, IOs stay idle	8.570	8.650	mA
4MHz	CPU, flash, SRAM, MCPWM, Timer, and all analog modules except PLL are active, IOs stay idle	3.012	3.165	mA
64kHz		2.445	2.618	mA
-	Deep Sleep Mode, PLL and BGP are turned off, only 64kHz LRC is running	27	30	uA
-	All analog modules	2.4	2.55	mA

Unless otherwise specified, the above tests are all measured at room temperature of 25°. Due to the deviation of the device model in the manufacturing process, the current consumption of different chips will have individual differences.

6 Analog Characteristics

Table 6-1 LKS32MC03x Analog Characteristics

Parameter	Min.	Typ.	Max.	Unit	Description
ADC					
Supply voltage	2.8	5	5.5	V	REF2VDD=0, ADC uses internal 2.4V reference
	2.4	5	5.5	V	REF2VDD=1, ADC uses AVDD as reference
Output bitrate		1.2		MHz	$f_{adc}/20$
Differential input signal range	-2.352		+2.352	V	REF2VDD=0, Gain=1; REF=2.4V
	-3.528		+3.528	V	REF2VDD=0, Gain=2/3; REF=3.6V
Single-ended input signal range	-0.3		+2.352	V	REF2VDD=0, Gain=1; REF=2.4V
	-0.3		+3.528	V	REF2VDD=0, Gain=2/3; REF=3.6V
	-0.3		AVDD*0.9	V	REF2VDD=1, Gain=1; REF=AVDD
	-0.3		AVDD+0.3	V	REF2VDD=1, Gain=2/3 , REF=AVDD, limited by IO diode clamp
The differential signal is usually the signal output from the OPA inside the chip to the ADC; The single-ended signal is usually the sampled signal from the external input through IO. Whether using an internal/external reference, the signal amplitude should not exceed ±98% of the ADC signal range. In particular, when using an external reference, it is recommended that the sampled signal not exceed 90% of the scale.					
DC offset		5	10	mV	Correctable
Effective number of bits (ENOB)	10.5	11		bit	
INL		2	3	LSB	
DNL		1	2	LSB	
SNR	63	66		dB	
Input resistance	500k			Ohm	
Input capacitance		10p		F	
Reference voltage (REF)					
Supply voltage	2.5	5	5.5	V	
Output deviation	-9		9	mV	
Power supply rejection ratio		70		dB	
Temperature coefficient		20		ppm/°C	

Parameter	Min.	Typ.	Max.	Unit	Description
Output voltage		2.4		V	
DAC					
Supply voltage	2.5	5	5.5	V	
Load resistance	50k			Ohm	
Load capacitance			50p	F	
Output voltage range	0.05		3.0	V	
Switching speed			1M	Hz	
DNL		1	2	LSB	
INL		2	4	LSB	
OFFSET		5	10	mV	
SNR	57	60	66	dB	
Operational amplifier (OPA)					
Supply voltage	3.1	5	5.5	V	
Bandwidth		10M	20M	Hz	
Load resistance	20k			Ohm	
Load capacitance			5p	F	
Common-mode input range	0		AVDD	V	
Output signal range	0.1		AVDD-0.1	V	Minimum load resistance
OFFSET		10	15	mV	This OFFSET is the equivalent differential input deviation obtained when the OPA differential input is short-circuited and OPA OUT is measured from 0 level. The output deviation of OPA is the OPA magnification x OFFSET
Common Mode Voltage (Vcm)	1.65		2.15	V	Measurement condition: normal temperature. Operational amplifier swing=2 × min(AVDD-Vcm, Vcm). It is recommended that the application using OPA single output should be powered on to measure Vcm and make software subtraction correction. For more analysis, please refer to the official website application note "ANN009 - Differences between Operational Amplifier Differential and Single Operating Mode".

Parameter	Min.	Typ.	Max.	Unit	Description
Common-mode rejection ratio (CMRR)		80		dB	
Power supply rejection ratio (PSRR)		80		dB	
Load current			500	uA	
Slew rate		5		V/us	
Phase margin		60		°	
Comparator (CMP)					
Supply voltage	2.5	5	5.5	V	
Input signal range	0		AVDD	V	
OFFSET		-12.92		mV	0 mV hysteresis, CMP output low-to-high inversion
		-12.12		mV	0 mV hysteresis, CMP output high-to-low inversion
		-11.63		mV	20 mV hysteresis, CMP output low-to-high inversion
		5.21		mV	20 mV hysteresis, CMP output high-to-low inversion
Transmission delay		0.15		uS	Default power consumption
		0.6		uS	Low power consumption
Hysteresis		20		mV	HYS='0'
		0		mV	HYS='1'
GPIO					
High Level Inversion Threshold	2.61		3.04	V	

Description of the analog register table:

The addresses 0x40000010-0x40000028 are the calibration registers for each module, which are provided with calibration values before being shipped from the factory. In general, you are not recommended to configure or change these values. To fine tune the analog parameters, you need to read the original calibration value.

The registers in the blank section must all be configured to 0 (reset to 0 when the chip is powered up). Other registers are configured as required by application scenarios.

7 Power Management System

The power management system consists of the LDO15 module and power-on/power-down reset module (POR).

7.1 Power Supply System for the AVDD Pin

For models 035D, 037E, and 037F, AVDD is the low-voltage power supply for the chip, with a power supply range of 2.5-5.5V. In applications where thermal conditions are good, it can be connected directly to the LDO5V pin of the chip. If an external DCDC or the 5V supply provided by a charge pump reduces system power consumption, this pin will be connected to an external 5V supply.

AVDD supplies power to the LDO15 module that powers all internal digital circuits and PLL modules.

LDO15 is automatically enabled after power-up and requires no software configuration, but the output voltage of LDO15 needs to be fine-tuned by software.

The output voltage of LDO15 can be adjusted by setting the register LDO15TRIM<2:0>. Please refer to the description of the analog register table for specific register values. LDO15 is calibrated before the chip is shipped from the factory, and generally, you do not need to configure these additional registers. To fine tune the output voltage of LDO, you need to read the original configuration value and fill in the configuration value corresponding to the fine-tuning amount.

The POR module monitors the voltage of LDO15 and provides a reset signal to the digital circuit when the LDO15 voltage falls below 1.1V (for example, at the beginning of power-up or during power-down), to avoid the abnormal operation of the digital circuit.

7.2 Power Supply System of the VCC Pin

For model 03x that is integrated with a 3P3N driver module, the VCC pin powers the on-chip driver module.

7.3 Power Supply System of the VCCLDO Pin

The VCCLDO pin powers the on-chip 5V LDO module. If 5V AVDD is used for external power supply, the power supply current is limited to below 30mA.

8 Timer System

The timer system consists of an internal 64kHz RC timer, an internal 4MHz RC timer, and a PLL circuit.

The 64k RC timer is used as an MCU slow timer, a filtration module or an MCU timer in a low power state. The 4MHz RC timer is used as the MCU master timer and, when used in conjunction with the PLL, it can provide a timer up to 48MHz.

The 64k and 4M RC timers are factory calibrated, the 4M RC timer has a customized calibration register to further calibrate the accuracy to ±0.5%. In the temperature range of -40-105℃, the accuracy of the 64k RC timer is ±50% and that of the 4M RC timer is ±1%.

The 64k RC timer frequency can be set with the register RCLTRIM <3:0>, and the 4M RC timer frequency can be set with the register RCHTRIM <5:0>, which corresponds to the values described in the analog register table.

The timer is calibrated before the chip is shipped from the factory, and generally, you do not need to configure these additional registers. To fine tune the frequency, you need to read the original configuration value and fill in the configuration value corresponding to the fine-tuning amount.

The 4M RC timer is turned on by setting RCHPD = '0' (on by default, and off when set to '1'). The RC timer requires the Bandgap voltage reference module to provide reference voltage and current. Therefore, it is necessary to enable the BGP module before turning on the RC timer. The 4M RC timer is turned on and the BGP module is enabled by default in case of chip power-up. The 64k RC timer is always turned on and cannot be turned off.

The PLL multiplies the frequency of the 4M RC timer, to ensure a higher-speed timer for modules such as MCU, ADC, etc. The highest timer of the MCU and PWM modules is 48MHz, while the typical timer of the ADC module is 24MHz.

The PLL module is enabled by setting PLLPDN = '1' (off by default, and on when set to 1). The BGP (Bandgap) module needs to be enabled before the PLL module. After enabling the PLL module, it will take a stabilization time of 6us to output a stable timer. By default when the chip is powered on, the RCH timer is turned on and the BGP module is enabled; however, the PLL module is disabled, and needs to be enabled with software.

9 Reference Voltage Source

The reference voltage source provides reference voltage and current for the ADC, DAC, RC timer, PLL, temperature sensor, operational amplifier, comparator, and FLASH. The reference voltage source of BGP needs to be enabled before using any of these modules.

The BGP module is enabled by default when the chip is powered on. The reference voltage source is enabled by setting BGPPD = '0', and BGP needs about 2us to stabilize from being enabled to disabled. The output voltage of BGP is about 1.2V with an accuracy of ±0.8%

10 ADC Module

A SAR ADC is integrated into the chip. The ADC module is disabled by default when the chip is powered on. Before the ADC is enabled, it is necessary to enable the BGP and PLL modules, turn on the 4M RC timer, and select the ADC operating frequency. The ADC operating timer is 24 M by default.

The ADC requires at least 17 ADC timer cycles to complete a conversion, of which 12 are conversion cycles and 5 are sampling ones. The sampling period can be set by configuring the SAMP_TIME register in SYS_AFE_REG2. It is required to set not less than 3 sampling periods, that is, more than 8 ADC clocks.

The recommended value is 3, which corresponds to an output data rate of 1.2MHz for the ADC.

The ADC operates in the following modes: single single-channel trigger, continuous single-channel trigger, single 1-16 channel scanning, and continuous 1-16 channel scanning. Each ADC has 16 independent sets of registers for each channel.

The ADC trigger event may come from external timer signals T0, T1, T2, T3 for a preset number of times, or may be triggered by software.

The ADC has two gain modes that are set by SYS_AFE_REG0.GA_AD, corresponding to 1 x time and 2/3 x times gains. The 1 x time gain corresponds to an input signal of ±2.4V, and the 2/3 x times gain corresponds to an input signal amplitude of ±3.6V. In measuring the output signal of an operational amplifier, the specific ADC gain is selected based on the maximum possible output signal of the operational amplifier.

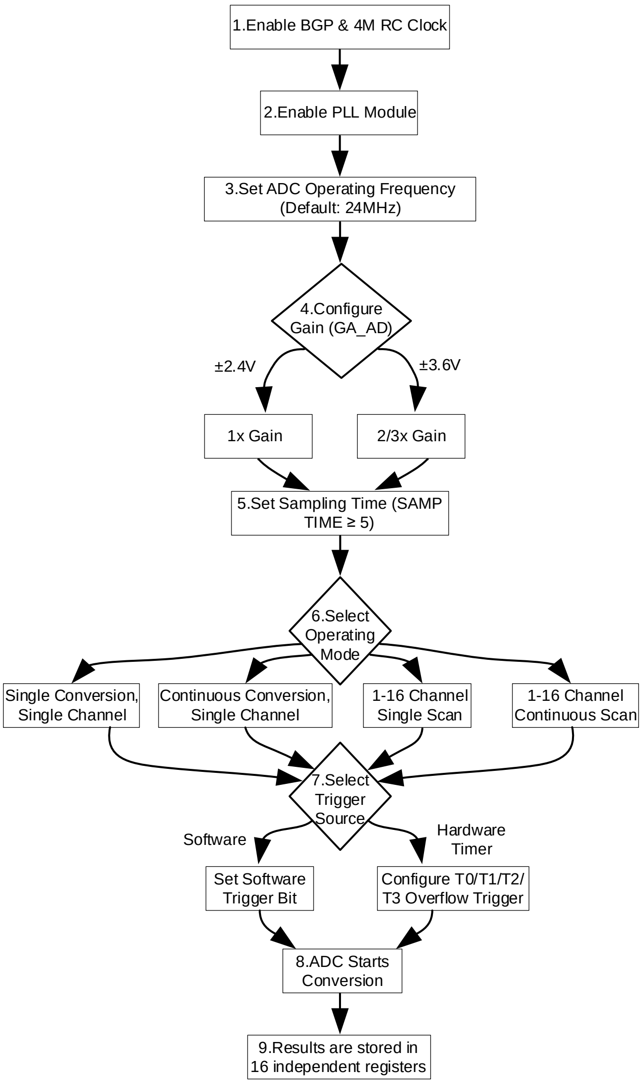

Figure 10-1ADC Configuration Flowchart

11 Operational Amplifier

Two input and output rail-to-rail operational amplifiers, with a built-in feedback resistor R2/R1. External pins should be connected in series with a resistor R0. The value of resistance of the feedback resistors R2:R1 can be set via register RES_OPA <1:0> for different magnification. The values corresponding to the specific registers are described in the analog register table.

The final magnification is R2/(R1+R0), where R0 is the value of resistance of the external resistor.

A capacitor greater than or equal to 15pF is required to be connected across the two input pins of the op amp.

For applications of direct sampling of MOS transistor resistor, it is recommended to connect an external resistor of >20kΩ to reduce the current flowing into the chip pins when the MOS transistor is turned off.

For small resistor sampling applications, external resistors of 100Ω are recommended.

The amplifier can select the output signal in the amplifier by setting OPAOUT_EN to send it to P0.7 IO port through BUFFER for measurement and application. Because BUFFER exists, it is also possible to send one output signal of the op amp under its normal operation mode.

In the default state when the chip is powered up, the amplifier module is turned off. The amplifier can be enabled by setting OPAPDN = '1' and the BGP module should be enabled before enabling the amplifier.

The clamping diode is built into the positive and negative input terminals of the op amp, and the motor phase line is directly connected to the input terminal through a matching resistor, thus simplifying the external circuit of MOSFET current sampling.

12 Comparator

There is a built-in 2 comparators, of which the comparison speed, the hysteresis voltage, and the signal source are programmable.

The comparator has a comparison delay of 0.15us and can also be set to less than 30ns via register CMP_FT. The hysteresis voltage is set to 20mV/0mV via CMP_HYS.

The signal source for both the positive and the negative inputs of the comparator can be programmed through the registers CMP_SELP<2:0> and CMP_SELN<1:0> as described in the register simulation instructions.

The comparator module is turned off by default when the chip is powered on. The comparator can be enabled by setting CMPxPDN ='1' and the BGP module should be enabled before enabling the comparator.

13 Temperature Sensor

A temperature sensor with an accuracy of ±2℃ is built into the chip. The chip will undergo temperature correction before delivery, and the correction value is saved in the flash info area.

The temperature sensor module is turned off by default when the chip is powered on. The BGP module should be enabled before enabling the temperature sensor.

The temperature sensor is turned on by setting TMPPDN = '1'. It takes approximately 2us to turn on until stable, so it needs to be turned on 2us before the ADC measures the sensor.

14 DAC Module

The chip has A built-in 8-bit DAC, and the output signal range of the A version is 3V, the output signal range of the B version is 3V/4.8V, and the output signal range of the C version is 1.2V/3V/4.8V.

For the C version of the chip, you need to set SYS AFE REG2.BIT15=1 to use the DAC's 1.2V range.

The 8bit DAC can be configured with register DACOUT EN=1 to send the DAC output to the IO port P0.0, which can drive a load resistance >50kΩ and a load capacitor of 50pF.

Since 03x series chips are not equipped with DAC hardware correction registers, in order to ensure DAC output accuracy, users need to read DACAMC/DACDC correction values of corresponding ranges from NVR according to different DAC ranges for software correction.

The digital quantity corresponding to the expected output value of the DAC is D_{DAC}, the gain correction is DAC_{AMC}, and the DC bias correction is DAC_{DC}. The DAC_{AMC} is a 10bit unsigned number, the $DAC_{AMC}[9]$ is an integer part, and the $DAC_{AMC}[8:0]$ is a decimal part, which can represent a fixed-point number near 1, and 0x200 corresponds to 1. The Saturation values are as follows:

SYS_AFE_DAC = Saturation(D_{DAC}*DAC_{AMC}-DAC_{DC})

See the official library function for details.

The maximum output bit rate of the DAC is 1MHz.

When the chip is powered on, the DAC module is disabled by default. The DAC can be enabled by setting DACPDN =1. Before enabling the DAC module, enable the BGP module.

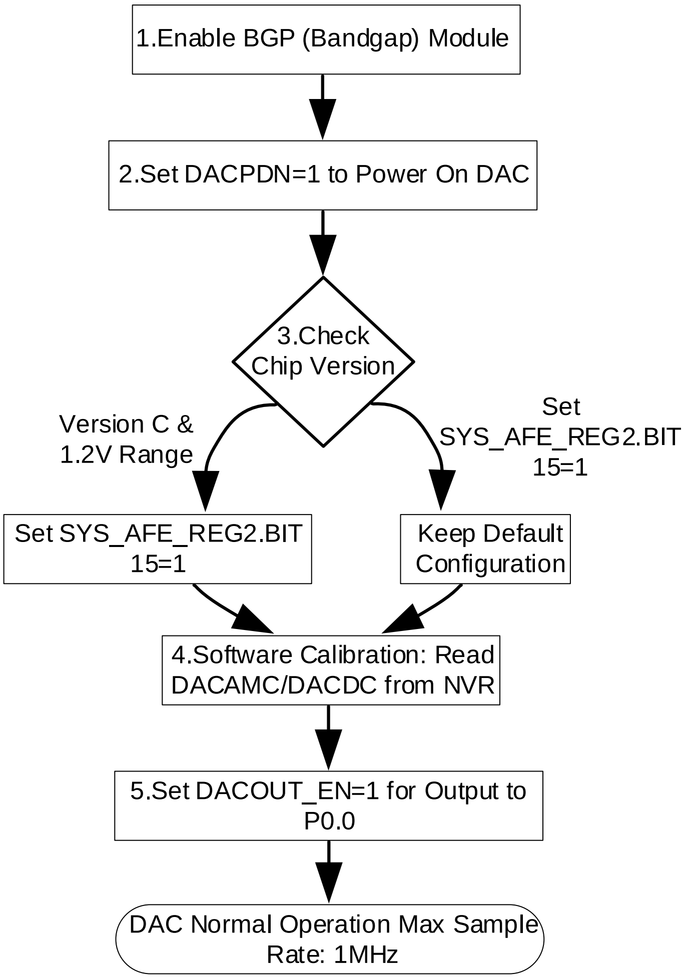

Figure 14-1DAC Configuration Flowchart

15 Processor

- 32-bit Cortex-M0 +DIV/SQRT coprocessor
- 2-wire SWD debugging pin
- Maximum operating frequency: 48MHz

16 Storage Resources

16.1 Flash

- The built-in flash includes a main storage area of 32kB and an information storage area of 1kB NVR
- Repeatable erasing and write-in of not less than 20,000 times
- Data is maintained for up to 100 years at a room temperature of 25℃
- The single-byte programming time is up to 7.5us, and the Sector erasing time is up to 5ms
- The Sector is 512 bytes, and can be erased or write-in by Sector. It supports runtime programming
- Flash data anti-theft (the last word must be written to any value other than 0xFFFFFFFF)

16.2 Execute-only Zone

Reprogramming with repeated erasure is supported.

16.3 SRAM

- Built-in 4KB SRAM

17 MCPWM Dedicated to Motor Drive

- The maximum operating timer frequency of MCPWM is 48MHz
- Supporting up to 4 channels complementary PWM outputs with adjustable phases
- The dead zone width of each channel can be configured independently
- Edge-aligned PWM mode supported
- Software control IO mode supported
- IO polarity control supported
- Internal short-circuit protection: avoiding short circuits caused by incorrect configuration
- External short-circuit protection: fast shutdown based on monitoring of external signals
- ADC sampling interrupt generates internally
- Use load register pre-memory timer to configure parameters
- The loading time and period of the loading register can be configured

18 Timer

- Two general-purpose timers, one 16bit timer and one 32bit timer
- Capturing mode is supported for measuring external signal width
- Comparison mode is supported for generating edge-aligned PWM/timing interrupts

19 Hall Sensor Interface

- Built-in maximum 1024 filtering
- Three Hall signal input
- 24-bit counter with overflow and capture interrupts

20 General Purpose Peripherals

- One UART works in the full-duplex operation mode, supporting 8/9 bits of data, 1/2 stop bit(s), odd/even/no parity mode, with 1 byte send cache, 1 byte receive cache, with Multi-drop Slave/Master mode, and the baud rate ranging from 300-115200
- One SPI for master-slave mode
- One IIC for master-slave mode
- Hardware watchdog, driven by RC timer, being independent of system high speed timer, write-in protection

21 Gate Drive Module

21.1 Module Parameters

The internal gate driver module of the chip has 2 different parameter specifications. According to the different gate driver circuit parameters, the gate driver module is divided into 2 models, which are G1 and G2 respectively. The comparison table is as 错误!未找到引用源。

In use, the LDO should not be pulled up before VCC is powered on, otherwise the LDO cannot be started after VCC is powered on.

Table 21-1 Device-Gate driver circuit version comparison table

Device	Gate Driver
LKS32MC031PC6Q8C	G2
LKS32MC035DL6S8(B/C)	G1
LKS32MC035EL6S8(B/C)	G2
LKS32MC037EM6S8(B/C)	G1
LKS32MC037FM6S8(B/C)	G2
LKS32MC037QM6Q8(B/C)	G1
LKS32MC037Q2M6Q8C	G2
LKS32MC039D2K6Q8C	G2
LKS32MC039DK6Q8B	G1

21.1.1 Gate Driver Module G1

Table 21-2 Gate Driver Module G1 parameter

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Static Parameter						
VCC	VCC voltage		7.5		32	V
VCC_ON	VCC undervoltage recovery voltage		5.8	6.5	7.4	V
VCC_UVLO	VCC undervoltage threshold voltage		5.4	6	6.8	V
VCC_HYS	Undervoltage voltage backlash		0.3	0.5	0.8	V
VHO	HOx (x = 1-3) output break-over voltage (since HO drives PMOS, low level corresponds to break-over)		VCC-11.5	VCC-10	VCC-8.5	V
V_{LO}	LOx (x=1-3) output		8.5	10	11.5	V

	break-over voltage					
I_{HO+}	HOx (x=1-3) input sink current	HOx=VCC	-	35	-	mA
I_{HO-}	HOx (x=1-3) output pull current	HOx=VCC-8V	-	300	-	mA
I_{LO+}	LOx (x=1-3) output pull current	LOx=0V	-	60	-	mA
I_{LO-}	LOx (x=1-3) input sink current	LOx=8V	-	300	-	mA
T_{SD}	TSD temperature		-	150	-	℃
$T_{RECOVER}$	TSD recovery temperature		-	135	-	℃
Operating temperature	Operating temperature of gate drive module		-40		105	℃
Junction temperature	Junction temperature of gate drive module				150	℃
I_{Ldo}	Power supply capacity			40		mA
Dynamic Parameter (CL = 1nF)						
T_{ON}	Break-over transmission delay		-	80	-	ns
T_{OFF}	Turn-off transmission delay		-	30	-	
TH_R	HOx rise time		-	60	-	
TH_F	HOx fall time		-	300	-	
TL_R	LOx rise time		-	300	-	
TH_F	LOx fall time		-	60	-	
DT	Built-in dead time		-	50	-	

Table 21-3 Gate Driver Module G1 5V LDO Module Parameter

5V LDO					
Input power	7.5		32	V	
Output voltage	4.75	5	5.25	V	+/-5% accuracy
Dropout voltage		2		V	
Output current		40		mA	
Ripple rejection		80		dB	
Decoupling capacitor input		0.33		uF	It is added to the VCCLDO pin. Please refer to the pin description section for details
Decoupling capacitor output		1		uF	It is added to the AVDD pin. Please refer to the pin description section for details
Operating temperature range	-40		125	℃	

21.1.2 Gate Driver Module G2

The gate drive modules integrated internally in 035E and 037F support low-power mode, while also integrating a supply voltage (VCC) sampling circuit. 035E and 031P can enter low-power mode by setting P0.4 output low level, turning off the output of gate drive, and turning off the supply voltage (VCC) sampling circuit. On the contrary, if you want the gate drive to output normally, you need to set P0.4 output high level. The switch for driving low power consumption mode of 037F is P0.3. The supply voltage (VCC) sampling channel of 035E is ADC_ CH3. The sampling channel for the supply voltage (VCC) of 037F is ADC_ CH1. The output voltage of the sampling circuit is VCC/15.

When G2 is in use, it is recommended that the VCC power-up rate be greater than 200 V/s to ensure proper startup of the LDO.

Table 21-1 Gate Driver Module G2 parameter

Symbol	**Parameter**	**Condition**	**Minimum**	**Typical**	**Maximum**	**Unit**
Static Parameter						
VCC	VCC voltage		5.7		32	V
VCC_ON	VCC undervoltage recovery voltage		4.8	5.2	5.6	V
VCC_UVLO	VCC undervoltage threshold voltage		4.4	4.8	5.2	V
VCC_HYS	Undervoltage voltage backlash		0.3	0.5	0.8	V
VHO	HOx (x = 1-3) output break-over voltage (since HO drives PMOS, low level corresponds to break-over)		VCC-11.5	VCC-10	VCC-8.5	V
V_{LO}	LOx (x=1-3) output break-over voltage		8.5	10	11.5	V
I_{HO+}	HOx (x=1-3) input sink current	HOx=VCC	-	35	-	mA
I_{HO-}	HOx (x=1-3) output pull current	HOx=VCC-8V	-	300	-	mA
I_{LO+}	LOx (x=1-3) output pull current	LOx=0V	-	60	-	mA
I_{LO-}	LOx (x=1-3) input sink current	LOx=8V	-	300	-	mA
T_{SD}	TSD temperature		-	160	-	°C
$T_{RECOVER}$	TSD recovery temperature		-	135	-	°C
I_{Ldo}	Power supply capacity			30		mA

Dynamic Parameter (CL = 1nF)						
T_{ON}	Break-over transmission delay		-	80	-	ns
T_{OFF}	Turn-off transmission delay		-	30	-	
TH_R	HOx rise time		-	50	-	
TH_F	HOx fall time		-	400	-	
TL_R	LOx rise time		-	200	-	
TH_F	LOx fall time		-	50	-	
DT	Built-in dead time		-	100	-	

Table 21-2 Gate Driver Module G2 5V LDO Module Parameter

5V LDO					
Input power	5.7		32	V	
Output voltage	4.55	4.95	5.35	V	
Dropout voltage		2		V	
Output current	0		30	mA	
LDO bypass capacity	1.0		10	uF	
Operating temperature range	-40		150	℃	

21.2 Recommended Application Diagram

The output pin signal LO1/HO1 of the driver module corresponds to the MCPWM function output of GPIO P0.10/P0.13, LO2/HO2 corresponds to the MCPWM function output of GPIO P0.11/P0.14, and LO3/HO3 corresponds to the MCPWM function output of GPIO P0.12/P0.15.

The MCPWM_SWAP register must be set for the integrated pre-drive chip, otherwise the PWM cannot be output normally. Write 0x67 to such register to write BIT[0] to 1, and write other values to write BIT[0] to 0. When the value of MCPWM_SWAP is 1, it is used to include the pre-drive chip application environment. The sequence is converted within the logic to facilitate the interconnection of the chip and the drive chip. In general applications, only three sets of MCPWM channels are required, so only three sets of sequences are converted.

21.2.1 3P3N Type Gate Drive Module

A 51ohm resistor is recommended between LO1/2/3 and the NMOS gate, HO1/2/3 and the PMOS gate when phase current is larger than 2A.

In applications where VCC is higher than 20V and the chip is not required to sleep, it is recommended to add a 1kΩ-2kΩ shunt resistor between VCC and AVDD, and this resistor is placed between the input and output of the internal 5V LDO to share part of the heat dissipation. The resistor must be placed at a distance from the chip.

The resistance value should be calculated according to the following formula:

$$R>=(VCC-AVDD)/I$$

Where, I is the total power dissipated on the 5V supply, including the power dissipated by the MCU and that dissipated by the 5V peripheral devices such as HALL.

With an external shunt resistor bridged, a 5.7V regulator should be placed at the AVDD pin.

At the same time, in the applications with a resistor between VCC and AVDD, it should be noted that the RC constant on RSTN should not be too large, and it is recommended to keep the RC constant at 1ms. That is, if there is no resistor outside the chip to 5V and the internal pull-up resistor is 100k, the capacitor on RSTN is selected as 10nF. If a 10k or 20k pull-up resistor is externally applied, the capacitor on RSTN is selected as 100nF.

There must be a decoupling capacitor higher than or equal to 10uF between the VCC pin and the ground.

The polarity of the gate drive module is as follows:

Table 21-3 Gate Drive Polarity Truth Table

{HIN, LIN}	HO	LO	
00	OFF	OFF	Shutdown of upper and lower tubes
01	OFF	ON	Lower tube conduction
10	ON	OFF	Upper tube conduction
11	OFF	OFF	The upper and lower tubes are connected simultaneously, and the hardware is under short-circuit protection

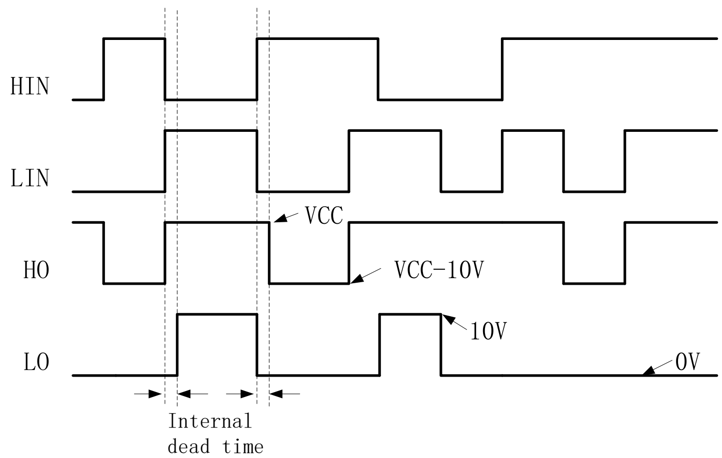

Figure 21-1 Schematic Diagram of Gate Drive Polarity

22 MOS

LKS32MC039PL5K6Q8B/LKS32MC039PL3K6Q8B/LKS32MC031PC6Q8C integrate a three-phase full bridge circuit composed of three pairs of MOS.

Table 22-8 LKS32MC039PL5K6Q8B MOS Parameter

Parameter		Min.	Typ.	Max.	Unit	Description
Output current (I_{OUT})			2		A	
On-state resistance	R_{DSON_N}		170		mΩ	VIN = 5V~24V， I_{OUT} = 0.5A~2A
	R_{DSON_P}		250			

Table 22-9 LKS32MC039PL3K6Q8B MOS Parameter

Parameter		Min.	Typ.	Max.	Unit	Description
Output current (I_{OUT})			1.5	2	A	
On-state resistance	R_{DSON_N}		170		mΩ	VIN = 4V， I_{OUT} = 1A~2A
	R_{DSON_P}		280			
	R_{DSON_N}		140			VIN = 9V， I_{OUT} = 1A~2A
	R_{DSON_P}		250			

LKS32MC039PL5K6Q8B/LKS32MC039PL3K6Q8B 驱动极性真值表

{DP | DN}	Power tube status	OUT status
00	Upper tube off, lower tube on	OUT low impedance to GND
11	Upper tube on, lower tube off	OUT Low Impedance to VCC
01	Upper tube off, lower tube off	OUT Output High Impedance
10	Upper tube on, lower tube on	Power tube straight-through, forbidden

Table 22-10 LKS32MC031PC6Q8 MOS Parameter

Parameter		Min.	Typ.	Max.	Unit	Description
NMOS sink current (I_{OUT})				6.5	A	
PMOS pull current (I_{OUT})		-4.4			A	
On-state resistance	R_{DSON_N}		20.2	27	mΩ	VGS = 4.5V, ID = 2A
	R_{DSON_P}		57	75.8		VGS =-4.5V, ID =-1.5A
	R_{DSON_N}		19.2	25		VGS = 10V, ID = 3A
	R_{DSON_P}		44	57.2		VGS =-10V, ID =-2A

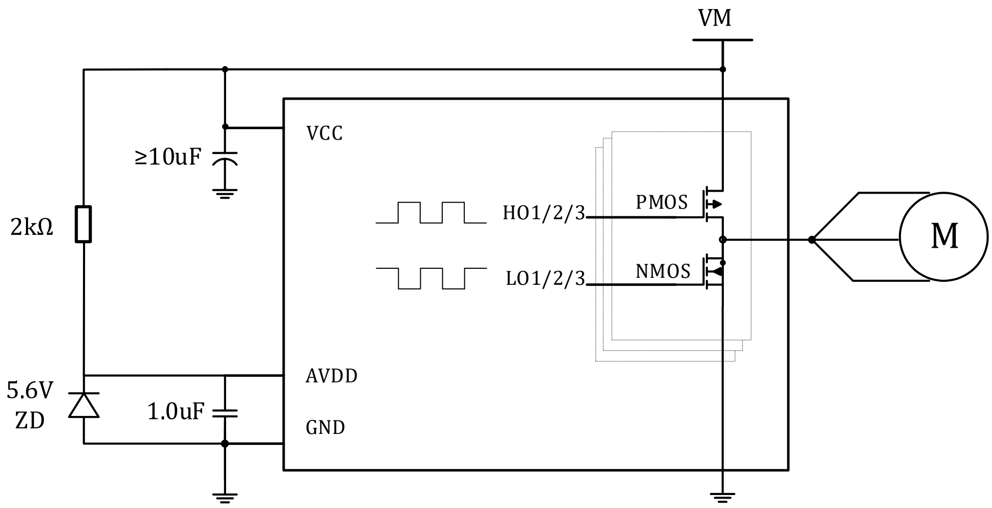

图 22-1 Typical Application Diagram of 3P3N Type Gate Drive Module

23 Special IO Multiplexing

Precautions for LKS03x special IO multiplexing

The SWD protocol consists of two signal lines: SWCLK and SWDIO. The former is a timer signal that, for the chip, is the input state and does not change the input state. The latter is a data signal that switches between an input state and an output state during data transmission for the chip, which defaults to the input state.

LKS03x can realize the function of multiplexing two IOs of SWD into other IOs. IO multiplexed by SWCLK is P1.8, and IO multiplexed by SWDIO is P1.9. The precautions are as follows:

- Multiplexing is disabled by default, and software is needed to write a 0 to SYS_IO_CFG[6] to enable the multiplexing. That is, after the hard reset of the chip is complete, the initial state is for SWD. The two IOs of the SWD have a pull-up inside the chip (the pull-up resistance of the chip is about 10K). When IO functions as SWD, the pull-up is turned on by default and cannot be turned off. When IO functions as GPIO, pull-up can be worked via GPIO1_PUE[8] and GPIO1_PUE[9]. P1.8 and P1.9 are fixed as SWD functions within 30ms of chip power-on reset, the software can write 0 to SYS_IO_CFG[6], but IO function switching takes effect after 30ms. LRC counting was used for 30ms with some deviation due to process reasons.
- When multiplexing is enabled, tools such as KEIL cannot directly access the chip, that is, Debug and erase download are unavailable. There are two options if you need to re-download the program.
- Firstly, it is recommended to use Linko dedicated offline downloader to erase. It is recommended to reserve a certain margin for the time for enabling software multiplexing, for example, approximately 100ms, to ensure that the offline downloader can be erased to prevent deadlock. The amount of margin is to ensure the success rate of offline downloader erasure. The larger the margin, the greater the probability of a successful one-time erase.
- Secondly, there is an exit mechanism inside the program. For example, the change of some other IO level (generally as input) indicates that the external needs to use SWDIO in software reconfiguration and de-multiplexing. At this point, the KEIL function can be restored.

In the packaging of SSOP24, QFN40, and SOP16L, SWDIO, SWCLK may have bonded with other IOs. At this point, it should be noted that other IO action may cause the chip to misinterpret the SWD action.

The considerations for SWCLK multiplexing are as follows:

- Multiplexing is disabled by default, and software is needed to enable the multiplexing. That is, after the hard reset of the chip, the initial state is used for SWCLK, which is pulled up inside the chip (the internal pull-up resistance of the chip is about 10K). Please pay attention if the initial level is required by the application.
- When multiplexing is enabled, tools such as KEIL cannot directly access the chip, that is, Debug and erase download are unavailable. There are two options if you need to re-download the program.

- Firstly, it is recommended to use Linko dedicated offline downloader to erase. It is recommended to reserve a certain margin for the time for enabling software multiplexing, for example, approximately 100ms, to ensure that the offline downloader can be erased to prevent deadlock. The amount of margin is to ensure the success rate of offline downloader erasure. The larger the margin, the greater the probability of a successful one-time erase.
- Second, there is an exit mechanism inside the program. For example, the change of some other IO level (generally as input) indicates that the external needs to use SWCLK in software reconfiguration and de-multiplexing. At this point, the KEIL function can be restored.

If only SWCLK is multiplexed and SWDIO is not multiplexed at this point, please refer to the above precautions.

RSTN signal is used for external reset pins for the LKS03x chip by default.

LKS03x can realize the functions of RSTN multiplexing into other IO. The multiplexed IO is P0.2. The precautions are as follows:

- Multiplexing is disabled by default, and software is needed to write a 1 to SYS_IO_CFG[5] to multiplex RSTN as a normal GPIO. That is, the initial state of the chip is used for RSTN, which is pulled up inside the chip (the internal pull-up resistance of the chip is about 100K). Please pay attention if the initial level is required by the application.
- The default state is RSTN. Program execution can only be started after RSTN is released normally. The application needs to ensure that RSTN has adequate protection, such as peripheral circuit pull-up. If capacitance can be added, it is better.
- When multiplexing is enabled, the RSTN function becomes invalid. If a hard reset of the chip is required, the source can only be powered down/watchdog.
- RSTN multiplexing does not affect the use of KEIL.

24 Ordering Information

Packaging types include Tray, Reel and Tube. The device quantity per package is determined by package type and package form, independent of device part number.

Tray Package:

Package Form	Quantity per Tray	Quantity per Inner Box	Quantity per Outer Carton
QFN 8×8	260 / Tray	2600 PCS	15600 PCS
QFN 4×4 / 5×5 / 6×6	490 / Tray	4900 PCS	29400 PCS
LQFP48 / TQFP48 0707	250 / Tray	2500 PCS	15000 PCS
LQFP64 1010	160 / Tray	1600 PCS	9600 PCS
LQFP100 1414	90 / Tray	900 PCS	5400 PCS
QFN5×6 48L-0.75	530 / Tray	5300 PCS	31800 PCS

Reel Packaging Information

Package Form	Quantity per Reel	Quantity per Inner Box	Quantity per Outer Carton
SOP16 / ESOP16L	3000 / Reel	6000 PCS	48000 PCS
SSOP24	4000 / Reel	8000 PCS	64000 PCS
QFN 3×3	5000 / Reel	5000 PCS	40000 PCS
TSSOP20 / 28	4000 / Reel	8000 PCS	64000 PCS

Tube Packaging Information

Package Form	Quantity per Tube	Quantity per Inner Box	Quantity per Outer Carton
SSOP24	50 / Tube	10000 PCS	4000 / 100000 PCS

Reel Package:

Package Type		Quantity per disc/tube	Quantity per box	Quantity boxes per case	Quantity per case
Braid -13 inches	SOP/ESOP8	4000	8000	8	64000
Braid -13 inches	SOP/ESOP16	3000	6000	8	48000
Braid -13 inches	SSOP24	4000	8000	8	64000
Braid -13 inches	TSSOP20	4000	8000	8	64000
Braid -13 inches	D/QFN3*3	5000	10000	8	80000
Braid -13 inches	D/QFN4*4	5000	10000	8	80000
Braid -13 inches	D/QFN5*5	5000	10000	8	80000
Pipe	SOP16	50	10000	10	100000
Pipe	SOP14/SSOP24	50	10000	10	100000
Pipe	TSSOP24	54	6480	6	38880

25 Version History

Table 25-1 Document Version History

Time	Version No.	Description
09/16/2026	3.04	Revise ADC channel count and sampling rate
08/25/2026	3.03	Revised Ordering Instructions
04/13/2026	3.02	Revise the flow chart of the ADC module
03/19/2026	3.01	Revise the chip model format in the Chip Model - Gate Drive Circuit Comparison Table
01/20/2026	3.00	Add ADC and DAC configuration flowchart
01/08/2026	2.99	Remove non-matching model types from the selection table.
01/07/2026	2.98	Revision of Operating Voltage for MC039D2K6Q8C
01/06/2026	2.97	Add model MC033PH6Q8C
12/24/2025	2.96	Remove the description of 16kB Flash from the storage section.
12/23/2025	2.96	LKS32MC034FLF6Q8B/C LKS32MC0342FLK6Q8C LKS32MC034SF6Q8(B/C) LKS32MC034S2F6Q8B/C LKS32MC034FLNK6Q8C Pre-driver supply voltage changed to 5-20V LKS32MC034F2LM6Q8C LKS32MC034F2LF6Q8C LKS32MC034F2LNK6Q8C LKS32MC034F2LN2K6Q8C Pre-driver supply voltage changed to 5-40V
11/19/2025	2.95	DK6Q8B Revised Package Diagram
10/13/2025	2.94	039PL5K6Q8B/C Schematic Diagram Revision
08/21/2025	2.93	Naming rule update
08/04/2025	2.92	Add LKS32MC039D2K6Q8C
07/31/2025	2.91	Supplementary SDA Pin Multiplexing
07/22/2025	2.90	Delete the Flash section: and simultaneous erasing of and write-in to one Sector can be made while reading and accessing another Sector
07/21/2025	2.89	Delete the description of the PVD module
05/15/2025	2.88	Gate drive module G2 LDO parameter update
05/13/2025	2.87	Added a description of the DAC configuration in the release notes section MC039PL5K6Q8B (C) Control Pin Information Correction MC039PL3K6Q8C Control Pin Information Correction MC039PL3K6Q8B Package size modification
04/11/2025	2.86	Add G2 module power-up speed
02/27/2025	2.84	Added MC039PL5 and MC039PL3 Truth Table
01/16/2025	2.83	Add Comparator flip voltage

11/28/2024	2.82	Update Vcc operating range of G1/G2, from 28V to 32V
11/21/2024	2.81	Description of Added ADC Saturation Range
11/11/2024	2.80	Device selection diagram modified
09/12/2024	2.79	Version No. synchronize Add instructions for use of pre-drive
09/19/2024	2.78	MOS information update
08/19/2024	2.77	Add pre-drive internal connection diagram
08/04/2024	2.76	Order package information updates to confirm package information by package type and package form
07/17/2024	2.75	Increase GPIO High Toggle Threshold and modify 031PC6Q8C pin definition
07/15/2024	2.74	031P pin assignment modified
07/04/2024	2.73	Update the operating temperature of MCU and driver module
06/04/2024	2.72	Update of electrical performance parameters
05/31/2024	2.71	LKS32MC031PC6Q8C PIN modified
05/29/2024	2.70	Add 031PC6Q8C
04/28/2024	2.69	Add 037Q2M6Q8C
04/10/2024	2.68	DAC description modified
04/02/2024	2.67	DAC adds description of software correction
03/20/2024	2.66	DAC added C version 1.2V range instructions
03/13/2024	2.65	Add C version description
02/20/2024	2.64	ESD data update
01/26/2024	2.63	Added 035E LDO module parameters
12/29/2023	2.62	035E/037F electrical performance parameter adjustment
12/12/2023	2.61	LKS32MC037FM6S8B PIN modified
11/09/2023	2.60	OPA OFFSET Adds the description, Renewal storage temperature
10/31/2023	2.59	VCC pin capacitance value revised
9/25/2023	2.58	Modified Pin temperature
7/28/2023	2.57	Add 038LY6Q8B
7/26/2023	2.56	Add DAC 1.2V range
6/4/2023	2.55	Add 035E and modify 037F pin distribution and parameters
5/23/2023	2.54	Delete 036D
4/11/2023	2.53	Modify package name
3/16/2023	2.52	Revise bits of data of UART
2/11/2023	2.51	Revise gate driver module G1 current parameter
2/8/2023	2.5	Revise 5V LDO input power
1/12/2023	2.49	Add characteristic of common mode voltage
1/9/2023	2.48	Add ordering information
11/28/2022	2.47	Revise the LRC clock frequency
11/24/2022	2.46	Revise 5V LDO output current
11/23/2022	2.45	Add 036D
11/21/2022	2.44	Update device selection table
11/12/2022	2.43	Update the LRC clock frequency and full temperature error range

11/7/2022	2.42	Add connection resistance between IO and internal analog circuit
10/28/2022	2.41	Add instructions for reading SYS_AFE_INFO to view chip version
10/25/2022	2.4	Revise name of version A/B
10/24/2022	2.31	Revise power supply
10/20/2022	2.3	Add 039D/039PL5/039PL3
10/12/2022	2.22	Add description of MCPWM_SWAP register
9/23/2022	2.21	Revise DateCode format
9/17/2022	2.2	Adjust 037Q Pin location
9/16/2022	2.11	034S has LDO inside.
9/6/2022	2.1	Add instructions of version A/B
8/11/2022	2.0	Split 3P3N, 6N and MCU model DS
7/27/2022	1.91	Add 034S
7/21/2022	1.9	Rollback ADC_CH6/7 pin position revision, the second revision time is tentatively scheduled for 2022.10
6/2/2022	1.8	Adjust ADC_CH6/7 Pin location, correct pin multiplexing table. DAC range is changed from 3.0V to 4.8V
3/8/2022	1.7	Add 034D
2/28/2022	1.6	Add 037Q
2/22/2022	1.5	Revise ADC channel number and CMP channel number, remove ADC_CH8 in pin function
1/24/2022	1.4	Revise P0.4, P0.6 Comparator 0 positive input number; Add P0.8 for 033
11/9/2021	1.3	Add 038
11/3/2021	1.2	Add 033, 037F
9/7/2021	1.1	Revised description for VCC power section
9/2/2021	1.0	Initial version

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