Linko Semiconductor Co., Ltd.

# *LKS32MC07X Datasheet*

# 1 Overview

## 1.1 Functions

LKS32MC07x is a 32-bit MCU targeting motor control applications, integrating all modules required by common motor control systems.

- **Features**
  - 96MHz 32-bit Cortex-M0 core
  - Customized instruction set DSP for motor control
  - Ultra low power sleep mode,10uA sleep current with MCU low low power consumption
  - Industrial temperature range
  - High ESD and group pulse reliability
- **Operating Conditions**
  - 2.5~5.5V power supply, with an integrated internal 5V LDO for partial power supply for internal MCU of chip
  - Operating Conditions: -40~105℃
- **Clock**
  - 8MHz built-in high-precision RC oscillator, with an accuracy of ± 1% at -40 ~ 105 ℃
  - 32KHz built-in low-speed clock for low-power mode
  - Operating on an external 8MHz crystal is available
  - Internal PLL up to 96 MHz
- **Flash**
  - Built-in flash including 64kB/128kB main area and 1.5kB NVR
  - Endurance: 100,000 Cycles(min)
  - Data retention: more than 100 years under room temperature 25 ℃
  - Single byte program: 7.5us(max), Sector erase: 5ms(max)
  - Sector size 512bytes, supporting Sector erase/program
  - Flash data anti-theft by programming the last word of flash to any words other than 0xFFFFFFFF
- **SRAM**
  - Built-in 12kB SRAM
- **Peripheral module**
  - Two UARTs
  - One SPI, support master-slave mode
  - One IIC, support master-slave mode
  - One CAN-bus (Some chips without CAN)
  - Two 16-bit standard timers (TIM), support capture and edge-aligned PWM function

- Two 32-bit standard timers (TIM), support capture and edge-aligned PWM function; support orthogonal code input, CW/CCW input, and pulse&symbol input
- Motor control PWM module, supports 12 channels/6 pairs of PWM waveform output, independent dead-band control
- Hall signal interface with speed measurement and debouncing function
- Hardware watchdog
- 4 Groups of 16bit GPIO at the most. 8 GPIOs could be used as wake-up source。15 GPIOs could be used as external IRQ source

- **Simulation module**
  - Two 12bit SAR ADC, simultaneous double sampling, 3Msps sampling and conversion rate, and each sampling circuit supports up to 16 channels, including 4 OPA outputs and 10 external ADC channels for a total of 14 optional ADC channel signals
  - Four operational amplifiers. Differential PGA mode is available.
  - Three comparators. Hysteresis mode is available.
  - Two 12bit digital-to-analog converter (DAC)
  - ± 2 ℃ built-in temperature sensor
  - 1.2V 0.8% built-in linear regulator
  - Low-power LDO and power monitoring circuit
  - RC oscillator with high precision and low temperature drift
  - Crystal oscillator circuits

## 1.2 Performance advantages

- High reliability, high integration level, small package size, saving BOM cost;
- Integrated 4 channels high-speed OPAs and 3 channels comparators, meeting the needs of different system topology like single resistance/double resistance/three resistance current sampling;
- High-speed OPA is integrated with over-voltage protection circuit, which allows high-voltage common-mode signals to be input, which could support direct current sampling of MOSFET resistance with the simplest circuit topology;
- Integrated hardware MOSFET temperature drift compensation circuit to ensure current sampling accuracy;
- Via a proprietary technique, ADC and high-speed OPA could cooperate well, making them able to handle a wider current dynamic range, while ensuring the sampling precision of high-speed small current and low-speed high current;
- The control circuit is simple and efficient, with strong anti-interference ability, stable and reliable;
- 2.5V~5.5V single power supply ensures the universality of system power supply;

- Supports IEC/UL60730 functional safety certification

Applicable to control systems such as inductive BLDC/non-inductive BLDC/inductive FOC/non-inductive FOC and stepper motors, permanent magnet synchronous and asynchronous motors.

## 1.3 Naming Conventions

**LKS32 MC 070 D 2 M 6 S 8 B (XX)**

**Device series**

| | |
|---|---|
| LKS32 | = 32bit MCU |
| LKS5 | = Gate Driver Products |
| LKS6 | = Power IC Product |

**Product type**

| | |
|---|---|
| MC | = Motor Control Applications |
| AT | = Automobile Applications |
| RV | = RISC-V for Motor Control |

**Device sub family**

| | |
|---|---|
| 070/071/075 | = 2.5~5.5V,2 ADC,4 PGA,DSP |
| 070FL/071DO/074D/DO | = 2.5~5.5V,2 ADC,4 PGA,DSP,6N Driver |
| 076/076F | = 2.5~5.5V,2 ADC,3 PGA,DSP,6N Driver |
| 072 | = 2.5~5.5V,2 ADC,3 PGA |
| 077 | = 2.5~5.5V,2 ADC,2 PGA |
| 077E | = 7.5~28V, 2 ADC,2 PGA,3P3N Driver |

**Gate Driver Functions**

| | |
|---|---|
| D | = 3P3N Gate Driver |
| E/DL | = 3P3N + 5V LDO |
| S/F | = 6N Gate Driver |
| SL/FL | = 6N + 5V LDO |
| K | = High V 6N Gate Driver |
| O/L5 | = 5V LDO/DCDC |
| L3 | = 3.3V/3V LDO |
| N | = DCDC |
| P | = 3P3N/4P4N DrMOS |
| Q | = 6N/8N DrMOS |
| PL3 | = 3P3N DrMOS + 3.3VLDO |
| PL5 | = 3P3N DrMOS + 5VLDO |
| QL | = 6N DrMOS + LDO |
| X | = PHY |
| XL | = PHY + LDO |

**PKG/Driver Ver**

| | |
|---|---|
| 2 | = 2nd Ver |
| S | = S 側面上锡 |

**Pin count**

| | |
|---|---|
| L | =16 pins |
| H | = 20 pins |
| M | = 24 pins |
| Y | =28 pins |
| K | = 32 pins |
| F | = 40 pins |
| G | = 42 pins |
| U | = 44 pins |
| C | = 48 pins |
| N | = 52 pins |
| S | = 54pins |
| E | = 60 pins |
| R | = 64 pins |
| P | = 80 pins |
| V | =100 pins |
| Q | =128 pins |
| Z | =144 pins |

**Code size**

| | |
|---|---|
| 4 | = 16Kbyte Flash Memory |
| 6 | = 32Kbyte Flash Memory |
| 8 | = 64Kbyte Flash Memory |
| B | =128Kbyte Flash Memory |
| C | =256Kbyte Flash Memory |
| D | =384Kbyte Flash Memory |
| E | =512Kbyte Flash Memory |

**Package**

| | |
|---|---|
| P | = TSSOP |
| T | = TQFP/LQFP |
| Q | = QFN |
| S | = SSOP |
| H | = BGA |

**Temperature range**

| | |
|---|---|
| 6 | = -40~85° |
| 8 | = -40~105° |
| 9 | = -40~125° |

**MCU Ver**

| | |
|---|---|
| B | = B ver |

**Options**

| | |
|---|---|
| TR | = Tape and reel packing |
| P | = ES |

Fig.1-1 Naming Conventions of Linko Components

## 1.4 Resource Diagram

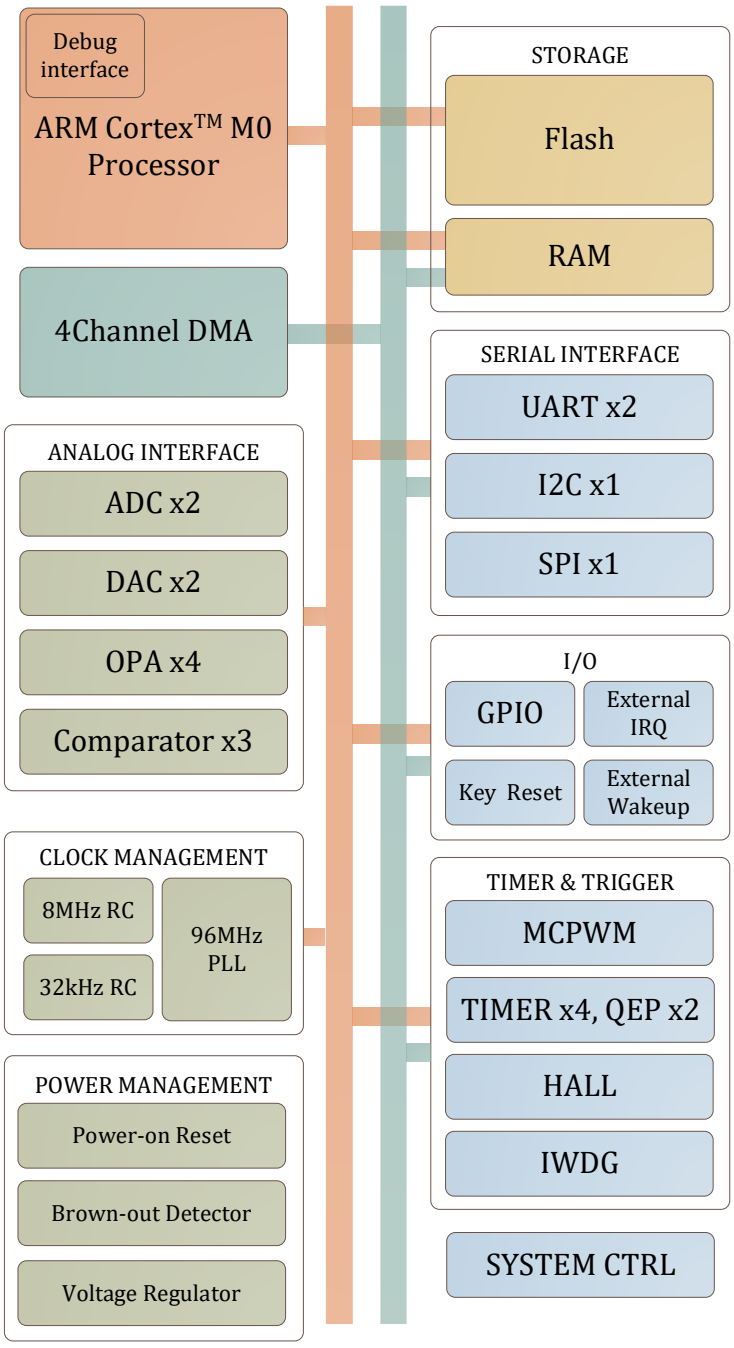
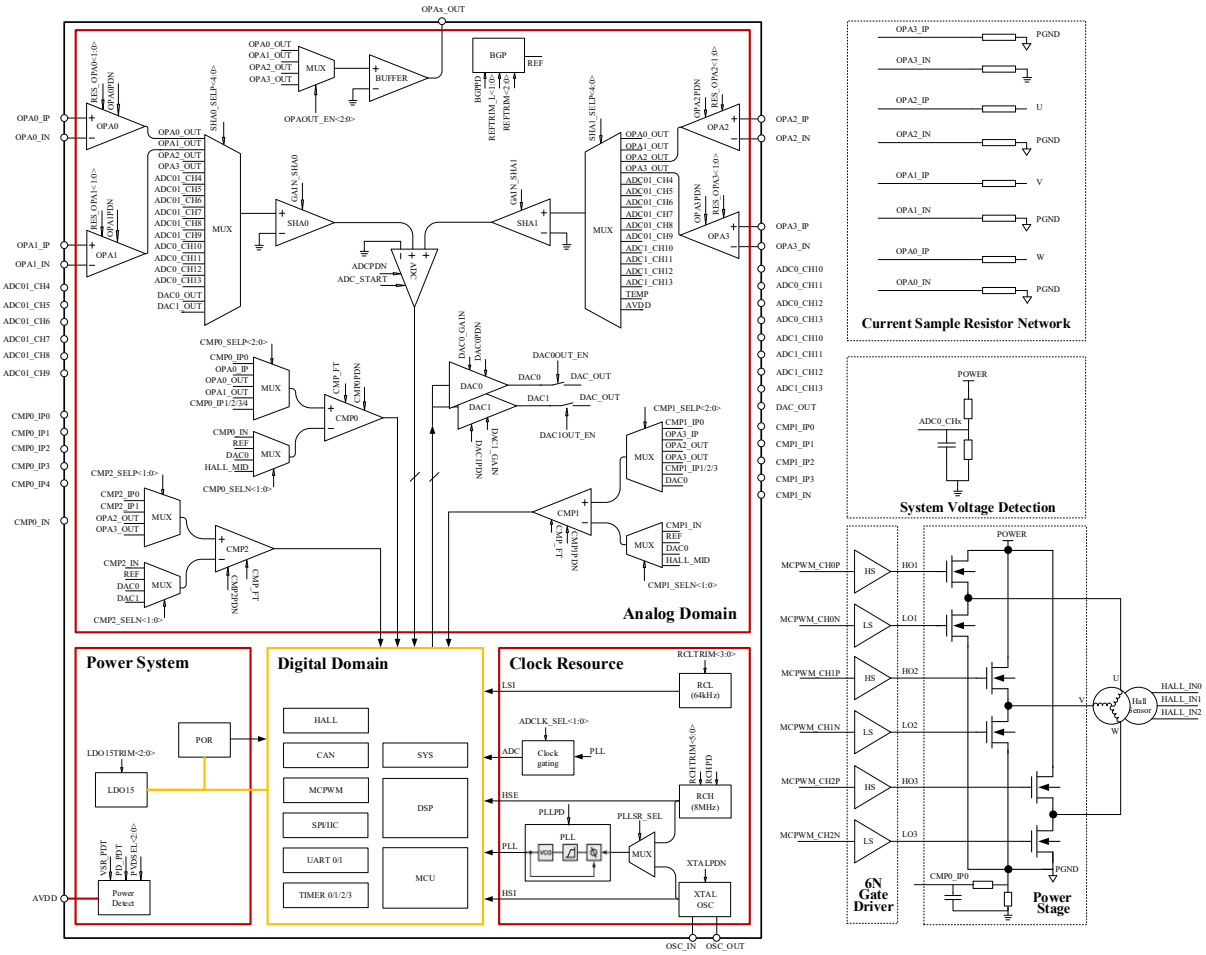



Fig.1-2 LKS32MC07x Resource Diagram

## 1.5 FOC System Example




* ADC 01 _ CH4 ~ ADC 01 _ CH9 are common channels for ADC0 and ADC 1

Fig.1-3 LKS32MC07x Simplified Schematic of FOC System

# 2 Device selection table

Table 2-1 LKS07x Series Device Selection Table

| | Frequency (MHz) | Flash (kB) | RAM (kB) | ADC ch. | DAC | Comparator | Comparator ch. | OPA | HALL | SPI | IIC | UART | CAN | Temp. Sensor | PLL | QEP | Gate driver | Gate Driver current (A) | Pre-drive supply (V) | Gate floating voltage (V) | Others | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LKS32MC070RBT8 | 96 | 128 | 12 | 14 | 12BITx2 | 3 | 11 | 4 | 3 | 1 | 1 | 2 | Yes | Yes | Yes | Yes | | | | | | LQFP64 |
| LKS32MC071CBT8 | 96 | 128 | 12 | 13 | 12BITx2 | 3 | 11 | 4 | 3 | 1 | 1 | 2 | Yes | Yes | Yes | Yes | | | | | | LQFP48、TQFP48 |
| LKS32MC071C8T8 | 96 | 64 | 12 | 13 | 12BITx2 | 3 | 11 | 4 | 3 | 1 | 1 | 2 | | Yes | Yes | Yes | | | | | | LQFP48、TQFP48 |
| LKS32MC072KBQ8 | 96 | 128 | 12 | 8 | 12BITx2 | 3 | 7 | 3 | 3 | 1 | 1 | 2 | | Yes | Yes | Yes | | | | | | QFN5*5 32L-0.75 |
| LKS32MC072KBT8 | 96 | 128 | 12 | 9 | 12BITx2 | 2 | 5 | 0 | 3 | 1 | 1 | 2 | Yes | Yes | Yes | Yes | | | | | | LQFP32 |
| LKS32MC073HBQ8 | 96 | 128 | 12 | 4 | 12BITx2 | 2 | 4 | 1 | 3 | 0 | 1 | 2 | Yes | Yes | Yes | Yes | | | | | | QFN3*3 20L-0.75 |
| LKS32MC077MBS8 | 96 | 64 | 12 | 6 | 12BITx2 | 3 | 6 | 2 | 3 | 1 | 1 | 2 | | Yes | Yes | Yes | | | | | | SSOP24L |

# 3 Pin Assignment

## 3.1 Pin Assignment and Pin Function Description

### 3.1.1 LKS32MC070RBT8


Fig.3-1 LKS32MC070RBT8 Pin Assignment

The red pin in the pin assignment figures below has built-in pull-up resistors:
RSTN has a 300kΩbuilt-in pull-up resistor, which is enabled automatically after power-up.
SWDIO/SWCLK has a 12kΩ built-in pull-up resistor, which is enabled automatically after power-up.
The remaining red pins have 12kΩ built-in pull-up resistors, which could be software-enabled.

Table 3-1 LKS32MC070RBT8 Pin Function Description

| | | |
|---|---|---|
| 1 | P0_0 | P0.0 |
| | CLKO | Clock output (for debugging) |
| | MCPWM_BKIN0 | PWM shutdown input signal 0 |
| | UART0_RXD | Serial port 0 receive (send) |
| | SPI_DI | SPI Data In (Out) |

| | | |
|---|---|---|
| | CLUOUT0 | CLU0 output |
| | ADC01_CH4 | ADC 0/ADC1 Channel 4 |
| | DAC0_OUT | DAC0 output |
| | DAC1_OUT | DAC1 Output |
| | FLT | IO filtering |
| | EXTI0 | External GPIO Interrupt Signal 0 |
| | WK0 | External wake-up signal 0 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 2 | P0_1 | P0.1 |
| | ADC01_CH6 | ADC 0/ADC1 Channel 6 |
| | EXTI1 | External GPIO Interrupt Signal 1 |
| 3 | P0_2 | P0.2 |
| | CLUOUT1 | CLU1 output |
| | RST_n | Reset pin, P0.2 used as RSTN by default. It is recommended to connect a 10 nF to 100 nF capacitor to ground and place a 12 K to 20 K pull-up resistor between RSTN and AVDD. If there is an external pull-up resistor, the capacitance of RSTN should be 100 nF. P0.2 can be switched as a GPIO, which turns off the 12 kΩ pull-up resistor. |
| | FLT | IO filtering |
| | EXTI2 | External GPIO Interrupt Signal 2 |
| | WK1 | External wake-up signal 1 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 4 | GND | Chip ground. It is strongly recommended that multiple ground pins be grounded uniformly on the PCB. |
| 5 | AVDD | Chip power supply, power supply range 2.5 ~ 5.5V |
| 6 | P3_2 | P3.2 |
| | MCPWM_CH3P | PWM Channel 3 High-Side |
| | CLUOUT2 | CLU2 output |
| 7 | P3_4 | P3.4 |
| | MCPWM_CH3N | PWM Channel 3 Low Side |
| 8 | P0_3 | P0.3 |
| | MCPWM_CH4P | PWM Channel 4 High Side |
| | SCL | I2C clock |
| | TIM2_CH0 | Timer2 channel 0 |
| | ADC01_CH7 | ADC0/ADC1 Channel 7 |
| | EXTI3 | External GPIO Interrupt Signal 3 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 9 | P0_4 | P0.4 |
| | MCPWM_CH4N | PWM Channel 4 Low Side |
| | SDA | I2C data |
| | TIM2_CH1 | Timer2 channel 1 |
| | ADC01_CH8 | ADC0/ADC1 Channel 8 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |

| | | |
|---|---|---|
| 10 | P0_5 | P0.5 |
| | HALL_IN0 | HALL interface input 0 |
| | MCPWM_CH5P | PWM Channel 5 High Side |
| | QEP0_Z | QEP0 Encoder Phase Z |
| | ADC01_CH9 | ADC0/ADC1 Channel 9 |
| 11 | P0_6 | P0.6 |
| | HALL_IN1 | HALL interface input 1 |
| | MCPWM_CH5N | PWM Channel 5 Low Side |
| | UART1_RXD | Serial port 1 receive (send) |
| | SCL | I2C clock |
| | TIM1_CH0 | Timer1 channel 0 |
| | CAN_RX | CAN receive |
| | CMP2_IN | Comparator 2 Negative Terminal Input |
| | FLT | IO filtering |
| | EXTI4 | External GPIO Interrupt 4 |
| | WK2 | External wake-up signal 2 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 12 | P0_7 | P0.7 |
| | HALL_IN2 | HALL interface input 2 |
| | MCPWM_BKIN1 | PWM Shutdown Input Signal 1 |
| | UART1_TXD | Serial port 1 send (receive) |
| | SDA | I2C data |
| | TIM1_CH1 | Timer1 channel 1 |
| | CAN_TX | Can sender |
| | CMP2_IP0 | Positive input 0 of comparator 2 |
| | FLT | IO filtering |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 13 | P1_1 | P1.1 |
| | SPI_CS | SPI chip select |
| | EXTI5 | External GPIO Interrupt 5 |
| 14 | P2_11 | P2.11 |
| | MCPWM_CH1P | PWM Channel 1 High Side |
| | TIM2_CH0 | Timer2 channel 0 |
| | CMP2_IP1 | Positive Input 1 of Comparator 2 |
| 15 | P2_12 | P2.12 |
| | MCPWM_CH1N | PWM Channel 1 Low Side |
| | SPI_CS | SPI chip select |
| | TIM2_CH1 | Timer2 channel 1 |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | CLUOUT3 | CLU3 output |
| | EXTI6 | External GPIO Interrupt 6 |
| 16 | P0_8 | P0.8 |
| 17 | P0_9 | P0.9 |

| | | |
|---|---|---|
| | SCL | I2C clock |
| | TIM2_CH0 | Timer2 channel 0 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 18 | P0_10 | P0.10 |
| | SDA | I2C data |
| | TIM2_CH1 | Timer2 channel 1 |
| 19 | P0_11 | P0.11 |
| | HALL_IN0 | HALL interface input 0 |
| | TIM3_CH0 | Timer3 channel 0 |
| | ADC1_CH11 | ADC1 Channel 11 |
| | CMP0_IP1 | Comparator 0 positive input 1 |
| | FLT | IO filtering |
| | EXTI7 | External GPIO Interrupt Signal 7 |
| | WK3 | External wake-up signal 3 |
| 20 | P0_12 | P0.12 |
| | HALL_IN1 | HALL interface input 1 |
| | TIM3_CH1 | Timer3 channel 1 |
| | CAN_RX | CAN receive |
| | ADC1_CH12 | ADC1 Channel 12 |
| | CMP0_IP2 | Comparator 0 positive input 2 |
| | FLT | IO filtering |
| 21 | P0_13 | P0.13 |
| | HALL_IN2 | HALL interface input 2 |
| | QEP0_Z | QEP0 Encoder Phase Z |
| | CAN_TX | Can sender |
| | ADC1_CH13 | ADC1 Channel 13 |
| | CMP0_IP3 | Comparator 0 positive input 3 |
| | FLT | IO filtering |
| 22 | P0_14 | P0.14 |
| | CMP0_OUT | Comparator 0 Output |
| | MCPWM_BKIN1 | PWM Shutdown Input Signal 1 |
| | UART0_TXD | Serial port 0 send (receive) |
| | SPI_CLK | SPI clock |
| | SCL | I2C clock |
| | TIM0_CH1 | Timer0 channel 1 |
| | QEP1_Z | Phase Z of QEP1 encoder |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | SIF | Single line communication |
| | CLUOUT0 | CLU0 output |
| | ADC0_CH10 | ADC0 Channel 10 |
| | CMP0_IP4 | Comparator 0 positive input 4 |
| | FLT | IO filtering |
| | EXTI8 | External GPIO Interrupt Signal 8 |

| | | |
|---|---|---|
| | WK4 | External wake-up signal 4 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 23 | P0_15 | P0.15 |
| | CMP2_OUT | Comparator 2 Output |
| | MCPWM_CH0P | PWM Channel 0 High Side |
| | UART0_RXD | Serial port 0 receive (send) |
| | SPI_DO | SPI Data Output (Input) |
| | SDA | I2C data |
| | TIM0_CH0 | Timer0 channel 0 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | CMP0_IN | Comparator 0 negative input |
| | FLT | IO filtering |
| | EXTI9 | External GPIO Interrupt 9 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 24 | P1_0 | P1.0 |
| | MCPWM_CH0N | PWM Channel 0 Low Side |
| | UART0_TXD | Serial port 0 send (receive) |
| | SPI_DI | SPI Data In (Out) |
| | TIM0_BKIN | TIMER0 _ FAIL signal from GPIO |
| | EXTI10 | External GPIO Interrupt Signal 10 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 25 | P3_6 | P3.6 |
| 26 | P1_2 | P1.2 |
| | TIM3_CH0 | Timer3 channel 0 |
| 27 | P1_3 | P1.3 |
| | TIM3_CH1 | Timer3 channel 1 |
| | ADC01_CH5 | ADC 0/ADC1 Channel 5 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 28 | P3_5 | P3.5 |
| | OPA0_IP | Positive terminal input of operational amplifier 0 |
| 29 | P3_7 | P3.7 |
| | OPA0_IN | Input of negative terminal of operational amplifier 0 |
| 30 | P2_7 | P2.7 |
| | CLKO | Clock output (for debugging) |
| | UART0_TXD | Serial port 0 send (receive) |
| | TIM0_CH0 | Timer0 channel 0 |
| | TIM3_CH1 | Timer3 channel 1 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | CAN_TX | Can sender |
| | CLUOUT1 | CLU1 output |
| | ADC0_CH11 | ADC0 Channel 11 |
| | OPAx_OUT | Op Amp Output |
| | LDO15 | 1.5V LDO Output |

| | | |
|---|---|---|
| | REF | Reference Voltage |
| | EXTI11 | External GPIO Interrupt Signal 11 |
| | WK6 | External wake-up signal 6 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 31 | P3_0 | P3.0 |
| | OPA1_IP | Positive input of operational amplifier 1 |
| 32 | P3_1 | P3.1 |
| | OPA1_IN | Op Amp 1 Negative Input |
| 33 | P2_8 | P2.8 |
| | UART1_RXD | Serial port 1 receive (send) |
| | SPI_DO | SPI Data Output (Input) |
| | TIM3_CH0 | Timer3 channel 0 |
| | OSC_IN | External crystal pin |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 34 | P3_9 | P3.9 |
| | UART1_TXD | Serial port 1 send (receive) |
| | TIM3_CH1 | Timer3 channel 1 |
| | OSC_OUT | External crystal pin |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 35 | P3_13 | P3.13 |
| 36 | P1_12 | P1.12 |
| 37 | P1_13 | P1.13 |
| | MCPWM_CH5P | PWM Channel 5 High Side |
| | SPI_CLK | SPI clock |
| | TIM0_CH0 | Timer0 channel 0 |
| 38 | P1_14 | P1.14 |
| | MCPWM_CH5N | PWM Channel 5 Low Side |
| | SPI_DO | SPI Data Output (Input) |
| | TIM0_CH1 | Timer0 channel 1 |
| 39 | P1_15 | P1.15 |
| | MCPWM_CH4P | PWM Channel 4 High Side |
| | SPI_DI | SPI Data In (Out) |
| | TIM2_CH0 | Timer2 channel 0 |
| 40 | P2_0 | P2.0 |
| | MCPWM_CH4N | PWM Channel 4 Low Side |
| | SPI_CS | SPI chip select |
| | TIM2_CH1 | Timer2 channel 1 |
| 41 | P1_4 | P1.4 |
| | MCPWM_CH0P | PWM Channel 0 High Side |
| | QEP0_Z | QEP0 Encoder Phase Z |
| 42 | P1_5 | P1.5 |
| | MCPWM_CH0N | PWM Channel 0 Low Side |
| 43 | P1_6 | P1.6 |

| | | |
|---|---|---|
| | MCPWM_CH1P | PWM Channel 1 High Side |
| 44 | P1_7 | P1.7 |
| | MCPWM_CH1N | PWM Channel 1 Low Side |
| 45 | P1_8 | P1.8 |
| | MCPWM_CH2P | PWM Channel 2 High Side |
| 46 | P1_9 | P1.9 |
| | MCPWM_CH2N | PWM Channel 2 Low Side |
| 47 | P1_10 | P1.10 |
| | MCPWM_CH3P | PWM Channel 3 High-Side |
| | UART0_RXD | Serial port 0 receive (send) |
| | SCL | I2C clock |
| | TIM0_CH0 | Timer0 channel 0 |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | ADC0_CH13 | ADC0 Channel 13 |
| | EXTI12 | External GPIO Interrupt Signal 12 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 48 | P1_11 | P1.11 |
| | MCPWM_CH3N | PWM Channel 3 Low Side |
| | UART0_TXD | Serial port 0 send (receive) |
| | SDA | I2C data |
| | TIM0_CH1 | Timer0 channel 1 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | SIF | Single line communication |
| | CLUOUT2 | CLU2 output |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 49 | P3_10 | P3.10 |
| | MCPWM_CH4P | PWM Channel 4 High Side |
| | OPA2_IP | Positive input of operational amplifier 2 |
| 50 | P3_11 | P3.11 |
| | MCPWM_CH4N | PWM Channel 4 Low Side |
| | OPA2_IN | Op Amp 2 Negative Input |
| 51 | P2_9 | P2.9 |
| | MCPWM_CH5P | PWM Channel 5 High Side |
| | SPI_DI | SPI Data In (Out) |
| | SCL | I2C clock |
| | ADC0_CH12 | ADC0 Channel 12 |
| | CMP0_IP0 | Comparator 0 positive input 0 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 52 | P2_10 | P2.10 |
| | MCPWM_CH5N | PWM Channel 5 Low Side |
| | SPI_DO | SPI Data Output (Input) |
| | SDA | I2C data |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |

| | | |
|---|---|---|
| 53 | P3_14 | P3.14 |
| | OPA3_IN | Op Amp 3 Negative Input |
| 54 | P3_15 | P3.15 |
| | OPA3_IP | Positive input of operational amplifier 3 |
| 55 | P2_1 | P2.1 |
| | SPI_CLK | SPI clock |
| | ADC1_CH10 | ADC1 Channel 10 |
| | CMP1_IP0 | Positive input 0 of comparator 1 |
| 56 | P3_12 | P3.12 |
| 57 | P2_2 | P2.2 |
| | QEP1_Z | Phase Z of QEP1 encoder |
| | CMP1_IN | Comparator 1 Negative Input |
| 58 | P2_3 | P2.3 |
| | CMP1_OUT | Comparator 1 Output |
| | MCPWM_BKIN0 | PWM shutdown input signal 0 |
| | SPI_CS | SPI chip select |
| | TIM0_CH1 | Timer0 channel 1 |
| | QEP0_Z | QEP0 Encoder Phase Z |
| | CLUOUT3 | CLU3 output |
| | FLT | IO filtering |
| | EXTI13 | External GPIO Interrupt Signal 13 |
| 59 | P2_4 | P2.4 |
| | CMP0_OUT | Comparator 0 Output |
| | HALL_IN0 | HALL interface input 0 |
| | MCPWM_CH2P | PWM Channel 2 High Side |
| | UART1_RXD | Serial port 1 receive (send) |
| | SPI_CLK | SPI clock |
| | TIM1_CH0 | Timer1 channel 0 |
| | TIM2_CH0 | Timer2 channel 0 |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | CAN_RX | CAN receive |
| | CMP1_IP1 | Comparator 1 positive input 1 |
| | FLT | IO filtering |
| | EXTI14 | External GPIO Interrupt Signal 14 |
| | WK5 | External wake-up signal 5 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 60 | P2_5 | P2.5 |
| | CMP1_OUT | Comparator 1 Output |
| | HALL_IN1 | HALL interface input 1 |
| | MCPWM_CH2N | PWM Channel 2 Low Side |
| | UART1_TXD | Serial port 1 send (receive) |
| | SPI_DO | SPI Data Output (Input) |
| | TIM1_CH1 | Timer1 channel 1 |

| | | |
|---|---|---|
| | TIM2_CH1 | Timer2 channel 1 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | CAN_TX | Can sender |
| | CMP1_IP2 | Comparator 1 positive input 2 |
| | FLT | IO filtering |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 61 | P2_6 | P2.6 |
| | CMP2_OUT | Comparator 2 Output |
| | HALL_IN2 | HALL interface input 2 |
| | MCPWM_CH3P | PWM Channel 3 High-Side |
| | TIM0_BKIN | TIMER0 _ FAIL signal from GPIO |
| | TIM3_CH0 | Timer3 channel 0 |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | SIF | Single line communication |
| | CLUOUT0 | CLU0 output |
| | CMP1_IP3 | Comparator 1 positive input 3 |
| | FLT | IO filtering |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 62 | P2_13 | P2.13 |
| | MCPWM_CH3N | PWM Channel 3 Low Side |
| | UART0_TXD | Serial port 0 send (receive) |
| | SPI_DO | SPI Data Output (Input) |
| | SCL | I2C clock |
| | TIM3_CH1 | Timer3 channel 1 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 63 | P2_14 | P2.14 |
| | SWCLK | SWD clock |
| | SPI_DI | SPI Data In (Out) |
| | SCL | I2C clock |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 64 | P2_15 | P2.15 |
| | SWDIO | SWD data |
| | UART0_RXD | Serial port 0 receive (send) |
| | SPI_CS | SPI chip select |
| | SDA | I2C data |
| | TIM2_CH1 | Timer2 channel 1 |
| | CLUOUT1 | CLU1 output |
| | EXTI15 | External GPIO Interrupt 15 |
| | WK7 | External wake-up signal 7 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |

### 3.1.2 LKS32MC071C8T8


Fig.3-2 LKS32MC071C8T8 Pin Assignment

* The red PIN pin in the figure has a built-in resistor that pulls up to AVDD:
The RSTN has an internal 300 kΩ pull-up resistor and is fixed on pull-up
SWDIO/SWCLK has a 12kΩ internal pull-up resistor and is fixed on pull-up.
The remaining red PIN pins have built-in 12 kΩ pull-up resistors, which can be turned on and off by software control.

Table3-2 LKS32MC071C8T8 Pin Function Description

| | | |
|---|---|---|
| 1 | P0_0 | P0.0 |
| | CLKO | Clock output (for debugging) |
| | MCPWM_BKIN0 | PWM shutdown input signal 0 |
| | UART0_RXD | Serial port 0 receive (send) |
| | SPI_DI | SPI Data In (Out) |
| | CLUOUT0 | CLU0 output |
| | ADC01_CH4 | ADC 0/ADC1 Channel 4 |
| | DAC0_OUT | DAC0 output |
| | DAC1_OUT | DAC1 Output |
| | FLT | IO filtering |

| | | |
|---|---|---|
| | EXTI0 | External GPIO Interrupt Signal 0 |
| | WK0 | External wake-up signal 0 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 2 | P0_2 | P0.2 |
| | CLUOUT1 | CLU1 output |
| | RST_n | Reset pin, P0.2 used as RSTN by default. It is recommended to connect a 10 nF to 100 nF capacitor to ground and place a 12 K to 20 K pull-up resistor between RSTN and AVDD. If there is an external pull-up resistor, the capacitance of RSTN should be 100 nF. P0.2 can be switched as a GPIO, which turns off the 12 kΩ pull-up resistor. |
| | FLT | IO filtering |
| | EXTI2 | External GPIO Interrupt Signal 2 |
| | WK1 | External wake-up signal 1 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 3 | GND | Chip ground. It is strongly recommended that multiple ground pins be grounded uniformly on the PCB. |
| 4 | AVDD | Chip power supply, power supply range 2.5 ~ 5.5V |
| 5 | P3_2 | P3.2 |
| | MCPWM_CH3P | PWM Channel 3 High-Side |
| | CLUOUT2 | CLU2 output |
| 6 | P0_3 | P0.3 |
| | MCPWM_CH4P | PWM Channel 4 High Side |
| | SCL | I2C clock |
| | TIM2_CH0 | Timer2 channel 0 |
| | ADC01_CH7 | ADC0/ADC1 Channel 7 |
| | EXTI3 | External GPIO Interrupt Signal 3 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 7 | P0_4 | P0.4 |
| | MCPWM_CH4N | PWM Channel 4 Low Side |
| | SDA | I2C data |
| | TIM2_CH1 | Timer2 channel 1 |
| | ADC01_CH8 | ADC0/ADC1 Channel 8 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 8 | P0_5 | P0.5 |
| | HALL_IN0 | HALL interface input 0 |
| | MCPWM_CH5P | PWM Channel 5 High Side |
| | QEP0_Z | QEP0 Encoder Phase Z |
| | ADC01_CH9 | ADC0/ADC1 Channel 9 |
| 9 | P0_6 | P0.6 |
| | HALL_IN1 | HALL interface input 1 |
| | MCPWM_CH5N | PWM Channel 5 Low Side |
| | UART1_RXD | Serial port 1 receive (send) |
| | SCL | I2C clock |

| | | |
|---|---|---|
| | TIM1_CH0 | Timer1 channel 0 |
| | CMP2_IN | Comparator 2 Negative Terminal Input |
| | FLT | IO filtering |
| | EXTI4 | External GPIO Interrupt 4 |
| | WK2 | External wake-up signal 2 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 10 | P0_7 | P0.7 |
| | HALL_IN2 | HALL interface input 2 |
| | MCPWM_BKIN1 | PWM Shutdown Input Signal 1 |
| | UART1_TXD | Serial port 1 send (receive) |
| | SDA | I2C data |
| | TIM1_CH1 | Timer1 channel 1 |
| | CMP2_IP0 | Positive input 0 of comparator 2 |
| | FLT | IO filtering |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 11 | P2_11 | P2.11 |
| | MCPWM_CH1P | PWM Channel 1 High Side |
| | TIM2_CH0 | Timer2 channel 0 |
| | CMP2_IP1 | Positive Input 1 of Comparator 2 |
| 12 | P2_12 | P2.12 |
| | MCPWM_CH1N | PWM Channel 1 Low Side |
| | SPI_CS | SPI chip select |
| | TIM2_CH1 | Timer2 channel 1 |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | CLUOUT3 | CLU3 output |
| | EXTI6 | External GPIO Interrupt 6 |
| 13 | P0_11 | P0.11 |
| | HALL_IN0 | HALL interface input 0 |
| | TIM3_CH0 | Timer3 channel 0 |
| | ADC1_CH11 | ADC1 Channel 11 |
| | CMP0_IP1 | Comparator 0 positive input 1 |
| | FLT | IO filtering |
| | EXTI7 | External GPIO Interrupt Signal 7 |
| | WK3 | External wake-up signal 3 |
| 14 | P0_12 | P0.12 |
| | HALL_IN1 | HALL interface input 1 |
| | TIM3_CH1 | Timer3 channel 1 |
| | ADC1_CH12 | ADC1 Channel 12 |
| | CMP0_IP2 | Comparator 0 positive input 2 |
| | FLT | IO filtering |
| 15 | P0_13 | P0.13 |
| | HALL_IN2 | HALL interface input 2 |
| | QEP0_Z | QEP0 Encoder Phase Z |

| | | |
|---|---|---|
| | ADC1_CH13 | ADC1 Channel 13 |
| | CMP0_IP3 | Comparator 0 positive input 3 |
| | FLT | IO filtering |
| 16 | P0_14 | P0.14 |
| | CMP0_OUT | Comparator 0 Output |
| | MCPWM_BKIN1 | PWM Shutdown Input Signal 1 |
| | UART0_TXD | Serial port 0 send (receive) |
| | SPI_CLK | SPI clock |
| | SCL | I2C clock |
| | TIM0_CH1 | Timer0 channel 1 |
| | QEP1_Z | Phase Z of QEP1 encoder |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | SIF | Single line communication |
| | CLUOUT0 | CLU0 output |
| | ADC0_CH10 | ADC0 Channel 10 |
| | CMP0_IP4 | Comparator 0 positive input 4 |
| | FLT | IO filtering |
| | EXTI8 | External GPIO Interrupt Signal 8 |
| | WK4 | External wake-up signal 4 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 17 | P0_15 | P0.15 |
| | CMP2_OUT | Comparator 2 Output |
| | MCPWM_CH0P | PWM Channel 0 High Side |
| | UART0_RXD | Serial port 0 receive (send) |
| | SPI_DO | SPI Data Output (Input) |
| | SDA | I2C data |
| | TIM0_CH0 | Timer0 channel 0 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | CMP0_IN | Comparator 0 negative input |
| | FLT | IO filtering |
| | EXTI9 | External GPIO Interrupt 9 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 18 | P1_0 | P1.0 |
| | MCPWM_CH0N | PWM Channel 0 Low Side |
| | UART0_TXD | Serial port 0 send (receive) |
| | SPI_DI | SPI Data In (Out) |
| | TIM0_BKIN | TIMER0 _ FAIL signal from GPIO |
| | EXTI10 | External GPIO Interrupt Signal 10 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 19 | P1_3 | P1.3 |
| | TIM3_CH1 | Timer3 channel 1 |
| | ADC01_CH5 | ADC 0/ADC1 Channel 5 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |

| | | |
|---|---|---|
| 20 | P3_5 | P3.5 |
| | OPA0_IP | Positive terminal input of operational amplifier 0 |
| 21 | P3_7 | P3.7 |
| | OPA0_IN | Input of negative terminal of operational amplifier 0 |
| 22 | P2_7 | P2.7 |
| | CLKO | Clock output (for debugging) |
| | UART0_TXD | Serial port 0 send (receive) |
| | TIM0_CH0 | Timer0 channel 0 |
| | TIM3_CH1 | Timer3 channel 1 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | CLUOUT1 | CLU1 output |
| | ADC0_CH11 | ADC0 Channel 11 |
| | OPAx_OUT | Op Amp Output |
| | LDO15 | 1.5V LDO Output |
| | REF | Reference Voltage |
| | EXTI11 | External GPIO Interrupt Signal 11 |
| | WK6 | External wake-up signal 6 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 23 | P3_0 | P3.0 |
| | OPA1_IP | Positive input of operational amplifier 1 |
| 24 | P3_1 | P3.1 |
| | OPA1_IN | Op Amp 1 Negative Input |
| 25 | P2_8 | P2.8 |
| | UART1_RXD | Serial port 1 receive (send) |
| | SPI_DO | SPI Data Output (Input) |
| | TIM3_CH0 | Timer3 channel 0 |
| | OSC_IN | External crystal pin |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 26 | P3_9 | P3.9 |
| | UART1_TXD | Serial port 1 send (receive) |
| | TIM3_CH1 | Timer3 channel 1 |
| | OSC_OUT | External crystal pin |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 27 | P1_4 | P1.4 |
| | MCPWM_CH0P | PWM Channel 0 High Side |
| | QEP0_Z | QEP0 Encoder Phase Z |
| 28 | P1_5 | P1.5 |
| | MCPWM_CH0N | PWM Channel 0 Low Side |
| 29 | P1_6 | P1.6 |
| | MCPWM_CH1P | PWM Channel 1 High Side |
| 30 | P1_7 | P1.7 |
| | MCPWM_CH1N | PWM Channel 1 Low Side |
| 31 | P1_8 | P1.8 |

| | | |
|---|---|---|
| | MCPWM_CH2P | PWM Channel 2 High Side |
| 32 | P1_9 | P1.9 |
| | MCPWM_CH2N | PWM Channel 2 Low Side |
| 33 | P1_10 | P1.10 |
| | MCPWM_CH3P | PWM Channel 3 High-Side |
| | UART0_RXD | Serial port 0 receive (send) |
| | SCL | I2C clock |
| | TIM0_CH0 | Timer0 channel 0 |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | ADC0_CH13 | ADC0 Channel 13 |
| | EXTI12 | External GPIO Interrupt Signal 12 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 34 | P1_11 | P1.11 |
| | MCPWM_CH3N | PWM Channel 3 Low Side |
| | UART0_TXD | Serial port 0 send (receive) |
| | SDA | I2C data |
| | TIM0_CH1 | Timer0 channel 1 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | SIF | Single line communication |
| | CLUOUT2 | CLU2 output |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 35 | P3_10 | P3.10 |
| | MCPWM_CH4P | PWM Channel 4 High Side |
| | OPA2_IP | Positive input of operational amplifier 2 |
| 36 | P3_11 | P3.11 |
| | MCPWM_CH4N | PWM Channel 4 Low Side |
| | OPA2_IN | Op Amp 2 Negative Input |
| 37 | P2_9 | P2.9 |
| | MCPWM_CH5P | PWM Channel 5 High Side |
| | SPI_DI | SPI Data In (Out) |
| | SCL | I2C clock |
| | CMP0_IP0 | Comparator 0 positive input 0 |
| | ADC0_CH12 | ADCO channel 12 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 38 | P2_10 | P2.10 |
| | MCPWM_CH5N | PWM Channel 5 Low Side |
| | SPI_DO | SPI Data Output (Input) |
| | SDA | I2C data |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 39 | P3_14 | P3.14 |
| | OPA3_IN | Op Amp 3 Negative Input |
| 40 | P3_15 | P3.15 |
| | OPA3_IP | Positive input of operational amplifier 3 |

| | | |
|---|---|---|
| 41 | P2_1 | P2.1 |
| | SPI_CLK | SPI clock |
| | ADC1_CH10 | ADC1 Channel 10 |
| | CMP1_IP0 | Positive input 0 of comparator 1 |
| 42 | P2_2 | P2.2 |
| | QEP1_Z | Phase Z of QEP1 encoder |
| | CMP1_IN | Comparator 1 Negative Input |
| 43 | P2_3 | P2.3 |
| | CMP1_OUT | Comparator 1 Output |
| | MCPWM_BKIN0 | PWM shutdown input signal 0 |
| | SPI_CS | SPI chip select |
| | TIM0_CH1 | Timer0 channel 1 |
| | QEP0_Z | QEP0 Encoder Phase Z |
| | CLUOUT3 | CLU3 output |
| | FLT | IO filtering |
| | EXTI13 | External GPIO Interrupt Signal 13 |
| 44 | P2_4 | P2.4 |
| | CMP0_OUT | Comparator 0 Output |
| | HALL_IN0 | HALL interface input 0 |
| | MCPWM_CH2P | PWM Channel 2 High Side |
| | UART1_RXD | Serial port 1 receive (send) |
| | SPI_CLK | SPI clock |
| | TIM1_CH0 | Timer1 channel 0 |
| | TIM2_CH0 | Timer2 channel 0 |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | CMP1_IP1 | Comparator 1 positive input 1 |
| | FLT | IO filtering |
| | EXTI14 | External GPIO Interrupt Signal 14 |
| | WK5 | External wake-up signal 5 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 45 | P2_5 | P2.5 |
| | CMP1_OUT | Comparator 1 Output |
| | HALL_IN1 | HALL interface input 1 |
| | MCPWM_CH2N | PWM Channel 2 Low Side |
| | UART1_TXD | Serial port 1 send (receive) |
| | SPI_DO | SPI Data Output (Input) |
| | TIM1_CH1 | Timer1 channel 1 |
| | TIM2_CH1 | Timer2 channel 1 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | CMP1_IP2 | Comparator 1 positive input 2 |
| | FLT | IO filtering |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 46 | P2_6 | P2.6 |

| | | |
|---|---|---|
| | CMP2_OUT | Comparator 2 Output |
| | HALL_IN2 | HALL interface input 2 |
| | MCPWM_CH3P | PWM Channel 3 High-Side |
| | TIM0_BKIN | TIMER0 _ FAIL signal from GPIO |
| | TIM3_CH0 | Timer3 channel 0 |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | SIF | Single line communication |
| | CLUOUT0 | CLU0 output |
| | CMP1_IP3 | Comparator 1 positive input 3 |
| | FLT | IO filtering |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 47 | P2_14 | P2.14 |
| | SWCLK | SWD clock |
| | SPI_DI | SPI Data In (Out) |
| | SCL | I2C clock |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 48 | P2_15 | P2.15 |
| | SWDIO | SWD data |
| | UART0_RXD | Serial port 0 receive (send) |
| | SPI_CS | SPI chip select |
| | SDA | I2C data |
| | TIM2_CH1 | Timer2 channel 1 |
| | CLUOUT1 | CLU1 output |
| | EXTI15 | External GPIO Interrupt 15 |
| | WK7 | External wake-up signal 7 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |

### 3.1.3 LKS32MC071CBT8


Fig.3-3 LKS32MC071CBT8 Pin Assignment

* The red PIN pin in the figure has a built-in resistor that pulls up to AVDD:
The RSTN has an internal 300 kΩ pull-up resistor and is fixed on pull-up
SWDIO/SWCLK has a 12kΩ internal pull-up resistor and is fixed on pull-up.
The remaining red PIN pins have built-in 12 kΩ pull-up resistors, which can be turned on and off by software control.

Table3-3 LKS32MC071CBT8 Pin Function Description

| | | |
|---|---|---|
| 1 | P0_0 | P0.0 |
| | CLKO | Clock output (for debugging) |
| | MCPWM_BKIN0 | PWM shutdown input signal 0 |
| | UART0_RXD | Serial port 0 receive (send) |
| | SPI_DI | SPI Data In (Out) |
| | CLUOUT0 | CLU0 output |
| | ADC01_CH4 | ADC 0/ADC1 Channel 4 |
| | DAC0_OUT | DAC0 output |
| | DAC1_OUT | DAC1 Output |
| | FLT | IO filtering |

| | | |
|---|---|---|
| | EXTI0 | External GPIO Interrupt Signal 0 |
| | WK0 | External wake-up signal 0 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 2 | P0_2 | P0.2 |
| | CLUOUT1 | CLU1 output |
| | RST_n | Reset pin, P0.2 used as RSTN by default. It is recommended to connect a 10 nF to 100 nF capacitor to ground and place a 12 K to 20 K pull-up resistor between RSTN and AVDD. If there is an external pull-up resistor, the capacitance of RSTN should be 100 nF. P0.2 can be switched as a GPIO, which turns off the 12 kΩ pull-up resistor. |
| | FLT | IO filtering |
| | EXTI2 | External GPIO Interrupt Signal 2 |
| | WK1 | External wake-up signal 1 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 3 | GND | Chip ground. It is strongly recommended that multiple ground pins be grounded uniformly on the PCB. |
| 4 | AVDD | Chip power supply, power supply range 2.5 ~ 5.5V |
| 5 | P3_2 | P3.2 |
| | MCPWM_CH3P | PWM Channel 3 High-Side |
| | CLUOUT2 | CLU2 output |
| 6 | P0_3 | P0.3 |
| | MCPWM_CH4P | PWM Channel 4 High Side |
| | SCL | I2C clock |
| | TIM2_CH0 | Timer2 channel 0 |
| | ADC01_CH7 | ADC0/ADC1 Channel 7 |
| | EXTI3 | External GPIO Interrupt Signal 3 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 7 | P0_4 | P0.4 |
| | MCPWM_CH4N | PWM Channel 4 Low Side |
| | SDA | I2C data |
| | TIM2_CH1 | Timer2 channel 1 |
| | ADC01_CH8 | ADC0/ADC1 Channel 8 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 8 | P0_5 | P0.5 |
| | HALL_IN0 | HALL interface input 0 |
| | MCPWM_CH5P | PWM Channel 5 High Side |
| | QEP0_Z | QEP0 Encoder Phase Z |
| | ADC01_CH9 | ADC0/ADC1 Channel 9 |
| 9 | P0_6 | P0.6 |
| | HALL_IN1 | HALL interface input 1 |
| | MCPWM_CH5N | PWM Channel 5 Low Side |
| | UART1_RXD | Serial port 1 receive (send) |
| | SCL | I2C clock |

| | | |
|---|---|---|
| | TIM1_CH0 | Timer1 channel 0 |
| | CAN_RX | CAN receive |
| | CMP2_IN | Comparator 2 Negative Terminal Input |
| | FLT | IO filtering |
| | EXTI4 | External GPIO Interrupt 4 |
| | WK2 | External wake-up signal 2 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 10 | P0_7 | P0.7 |
| | HALL_IN2 | HALL interface input 2 |
| | MCPWM_BKIN1 | PWM Shutdown Input Signal 1 |
| | UART1_TXD | Serial port 1 send (receive) |
| | SDA | I2C data |
| | TIM1_CH1 | Timer1 channel 1 |
| | CAN_TX | Can sender |
| | CMP2_IP0 | Positive input 0 of comparator 2 |
| | FLT | IO filtering |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 11 | P2_11 | P2.11 |
| | MCPWM_CH1P | PWM Channel 1 High Side |
| | TIM2_CH0 | Timer2 channel 0 |
| | CMP2_IP1 | Positive Input 1 of Comparator 2 |
| 12 | P2_12 | P2.12 |
| | MCPWM_CH1N | PWM Channel 1 Low Side |
| | SPI_CS | SPI chip select |
| | TIM2_CH1 | Timer2 channel 1 |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | CLUOUT3 | CLU3 output |
| | EXTI6 | External GPIO Interrupt 6 |
| 13 | P0_11 | P0.11 |
| | HALL_IN0 | HALL interface input 0 |
| | TIM3_CH0 | Timer3 channel 0 |
| | ADC1_CH11 | ADC1 Channel 11 |
| | CMP0_IP1 | Comparator 0 positive input 1 |
| | FLT | IO filtering |
| | EXTI7 | External GPIO Interrupt Signal 7 |
| | WK3 | External wake-up signal 3 |
| 14 | P0_12 | P0.12 |
| | HALL_IN1 | HALL interface input 1 |
| | TIM3_CH1 | Timer3 channel 1 |
| | ADC1_CH12 | ADC1 Channel 12 |
| | CAN_RX | CAN receive |
| | CMP0_IP2 | Comparator 0 positive input 2 |
| | FLT | IO filtering |

| | | |
|---|---|---|
| 15 | P0_13 | P0.13 |
| | HALL_IN2 | HALL interface input 2 |
| | QEP0_Z | QEP0 Encoder Phase Z |
| | ADC1_CH13 | ADC1 Channel 13 |
| | CAN_TX | CAN sender |
| | CMP0_IP3 | Comparator 0 positive input 3 |
| | FLT | IO filtering |
| 16 | P0_14 | P0.14 |
| | CMP0_OUT | Comparator 0 Output |
| | MCPWM_BKIN1 | PWM Shutdown Input Signal 1 |
| | UART0_TXD | Serial port 0 send (receive) |
| | SPI_CLK | SPI clock |
| | SCL | I2C clock |
| | TIM0_CH1 | Timer0 channel 1 |
| | QEP1_Z | Phase Z of QEP1 encoder |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | SIF | Single line communication |
| | CLUOUT0 | CLU0 output |
| | ADC0_CH10 | ADC0 Channel 10 |
| | CMP0_IP4 | Comparator 0 positive input 4 |
| | FLT | IO filtering |
| | EXTI8 | External GPIO Interrupt Signal 8 |
| | WK4 | External wake-up signal 4 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 17 | P0_15 | P0.15 |
| | CMP2_OUT | Comparator 2 Output |
| | MCPWM_CH0P | PWM Channel 0 High Side |
| | UART0_RXD | Serial port 0 receive (send) |
| | SPI_DO | SPI Data Output (Input) |
| | SDA | I2C data |
| | TIM0_CH0 | Timer0 channel 0 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | CMP0_IN | Comparator 0 negative input |
| | FLT | IO filtering |
| | EXTI9 | External GPIO Interrupt 9 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 18 | P1_0 | P1.0 |
| | MCPWM_CH0N | PWM Channel 0 Low Side |
| | UART0_TXD | Serial port 0 send (receive) |
| | SPI_DI | SPI Data In (Out) |
| | TIM0_BKIN | TIMER0 _ FAIL signal from GPIO |
| | EXTI10 | External GPIO Interrupt Signal 10 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |

| | | |
|---|---|---|
| 19 | P1_3 | P1.3 |
| | TIM3_CH1 | Timer3 channel 1 |
| | ADC01_CH5 | ADC 0/ADC1 Channel 5 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 20 | P3_5 | P3.5 |
| | OPA0_IP | Positive terminal input of operational amplifier 0 |
| 21 | P3_7 | P3.7 |
| | OPA0_IN | Input of negative terminal of operational amplifier 0 |
| 22 | P2_7 | P2.7 |
| | CLKO | Clock output (for debugging) |
| | UART0_TXD | Serial port 0 send (receive) |
| | TIM0_CH0 | Timer0 channel 0 |
| | TIM3_CH1 | Timer3 channel 1 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | CAN_TX | CAN sender |
| | CLUOUT1 | CLU1 output |
| | ADC0_CH11 | ADC0 Channel 11 |
| | OPAx_OUT | Op Amp Output |
| | LDO15 | 1.5V LDO Output |
| | REF | Reference Voltage |
| | EXTI11 | External GPIO Interrupt Signal 11 |
| | WK6 | External wake-up signal 6 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 23 | P3_0 | P3.0 |
| | OPA1_IP | Positive input of operational amplifier 1 |
| 24 | P3_1 | P3.1 |
| | OPA1_IN | Op Amp 1 Negative Input |
| 25 | P2_8 | P2.8 |
| | UART1_RXD | Serial port 1 receive (send) |
| | SPI_DO | SPI Data Output (Input) |
| | TIM3_CH0 | Timer3 channel 0 |
| | OSC_IN | External crystal pin |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 26 | P3_9 | P3.9 |
| | UART1_TXD | Serial port 1 send (receive) |
| | TIM3_CH1 | Timer3 channel 1 |
| | OSC_OUT | External crystal pin |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 27 | P1_4 | P1.4 |
| | MCPWM_CH0P | PWM Channel 0 High Side |
| | QEP0_Z | QEP0 Encoder Phase Z |
| 28 | P1_5 | P1.5 |
| | MCPWM_CH0N | PWM Channel 0 Low Side |

| | | |
|---|---|---|
| 29 | P1_6 | P1.6 |
| | MCPWM_CH1P | PWM Channel 1 High Side |
| 30 | P1_7 | P1.7 |
| | MCPWM_CH1N | PWM Channel 1 Low Side |
| 31 | P1_8 | P1.8 |
| | MCPWM_CH2P | PWM Channel 2 High Side |
| 32 | P1_9 | P1.9 |
| | MCPWM_CH2N | PWM Channel 2 Low Side |
| 33 | P1_10 | P1.10 |
| | MCPWM_CH3P | PWM Channel 3 High-Side |
| | UART0_RXD | Serial port 0 receive (send) |
| | SCL | I2C clock |
| | TIM0_CH0 | Timer0 channel 0 |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | ADC0_CH13 | ADC0 Channel 13 |
| | EXTI12 | External GPIO Interrupt Signal 12 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 34 | P1_11 | P1.11 |
| | MCPWM_CH3N | PWM Channel 3 Low Side |
| | UART0_TXD | Serial port 0 send (receive) |
| | SDA | I2C data |
| | TIM0_CH1 | Timer0 channel 1 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | SIF | Single line communication |
| | CLUOUT2 | CLU2 output |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 35 | P3_10 | P3.10 |
| | MCPWM_CH4P | PWM Channel 4 High Side |
| | OPA2_IP | Positive input of operational amplifier 2 |
| 36 | P3_11 | P3.11 |
| | MCPWM_CH4N | PWM Channel 4 Low Side |
| | OPA2_IN | Op Amp 2 Negative Input |
| 37 | P2_9 | P2.9 |
| | MCPWM_CH5P | PWM Channel 5 High Side |
| | SPI_DI | SPI Data In (Out) |
| | SCL | I2C clock |
| | CMP0_IP0 | Comparator 0 positive input 0 |
| | ADC0_CH12 | ADCO channel 12 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 38 | P2_10 | P2.10 |
| | MCPWM_CH5N | PWM Channel 5 Low Side |
| | SPI_DO | SPI Data Output (Input) |
| | SDA | I2C data |

| | | |
|---|---|---|
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 39 | P3_14 | P3.14 |
| | OPA3_IN | Op Amp 3 Negative Input |
| 40 | P3_15 | P3.15 |
| | OPA3_IP | Positive input of operational amplifier 3 |
| 41 | P2_1 | P2.1 |
| | SPI_CLK | SPI clock |
| | ADC1_CH10 | ADC1 Channel 10 |
| | CMP1_IP0 | Positive input 0 of comparator 1 |
| 42 | P2_2 | P2.2 |
| | QEP1_Z | Phase Z of QEP1 encoder |
| | CMP1_IN | Comparator 1 Negative Input |
| 43 | P2_3 | P2.3 |
| | CMP1_OUT | Comparator 1 Output |
| | MCPWM_BKIN0 | PWM shutdown input signal 0 |
| | SPI_CS | SPI chip select |
| | TIM0_CH1 | Timer0 channel 1 |
| | QEP0_Z | QEP0 Encoder Phase Z |
| | CLUOUT3 | CLU3 output |
| | FLT | IO filtering |
| | EXTI13 | External GPIO Interrupt Signal 13 |
| 44 | P2_4 | P2.4 |
| | CMP0_OUT | Comparator 0 Output |
| | HALL_IN0 | HALL interface input 0 |
| | MCPWM_CH2P | PWM Channel 2 High Side |
| | UART1_RXD | Serial port 1 receive (send) |
| | SPI_CLK | SPI clock |
| | TIM1_CH0 | Timer1 channel 0 |
| | TIM2_CH0 | Timer2 channel 0 |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | CAN_RX | CAN receive |
| | CMP1_IP1 | Comparator 1 positive input 1 |
| | FLT | IO filtering |
| | EXTI14 | External GPIO Interrupt Signal 14 |
| | WK5 | External wake-up signal 5 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 45 | P2_5 | P2.5 |
| | CMP1_OUT | Comparator 1 Output |
| | HALL_IN1 | HALL interface input 1 |
| | MCPWM_CH2N | PWM Channel 2 Low Side |
| | UART1_TXD | Serial port 1 send (receive) |
| | SPI_DO | SPI Data Output (Input) |
| | TIM1_CH1 | Timer1 channel 1 |

| | | |
|---|---|---|
| | TIM2_CH1 | Timer2 channel 1 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | CAN_TX | CAN sender |
| | CMP1_IP2 | Comparator 1 positive input 2 |
| | FLT | IO filtering |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 46 | P2_6 | P2.6 |
| | CMP2_OUT | Comparator 2 Output |
| | HALL_IN2 | HALL interface input 2 |
| | MCPWM_CH3P | PWM Channel 3 High-Side |
| | TIM0_BKIN | TIMER0 _ FAIL signal from GPIO |
| | TIM3_CH0 | Timer3 channel 0 |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | SIF | Single line communication |
| | CLUOUT0 | CLU0 output |
| | CMP1_IP3 | Comparator 1 positive input 3 |
| | FLT | IO filtering |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 47 | P2_14 | P2.14 |
| | SWCLK | SWD clock |
| | SPI_DI | SPI Data In (Out) |
| | SCL | I2C clock |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 48 | P2_15 | P2.15 |
| | SWDIO | SWD data |
| | UART0_RXD | Serial port 0 receive (send) |
| | SPI_CS | SPI chip select |
| | SDA | I2C data |
| | TIM2_CH1 | Timer2 channel 1 |
| | CLUOUT1 | CLU1 output |
| | EXTI15 | External GPIO Interrupt 15 |
| | WK7 | External wake-up signal 7 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |

### 3.1.4 LKS32MC072KBQ8

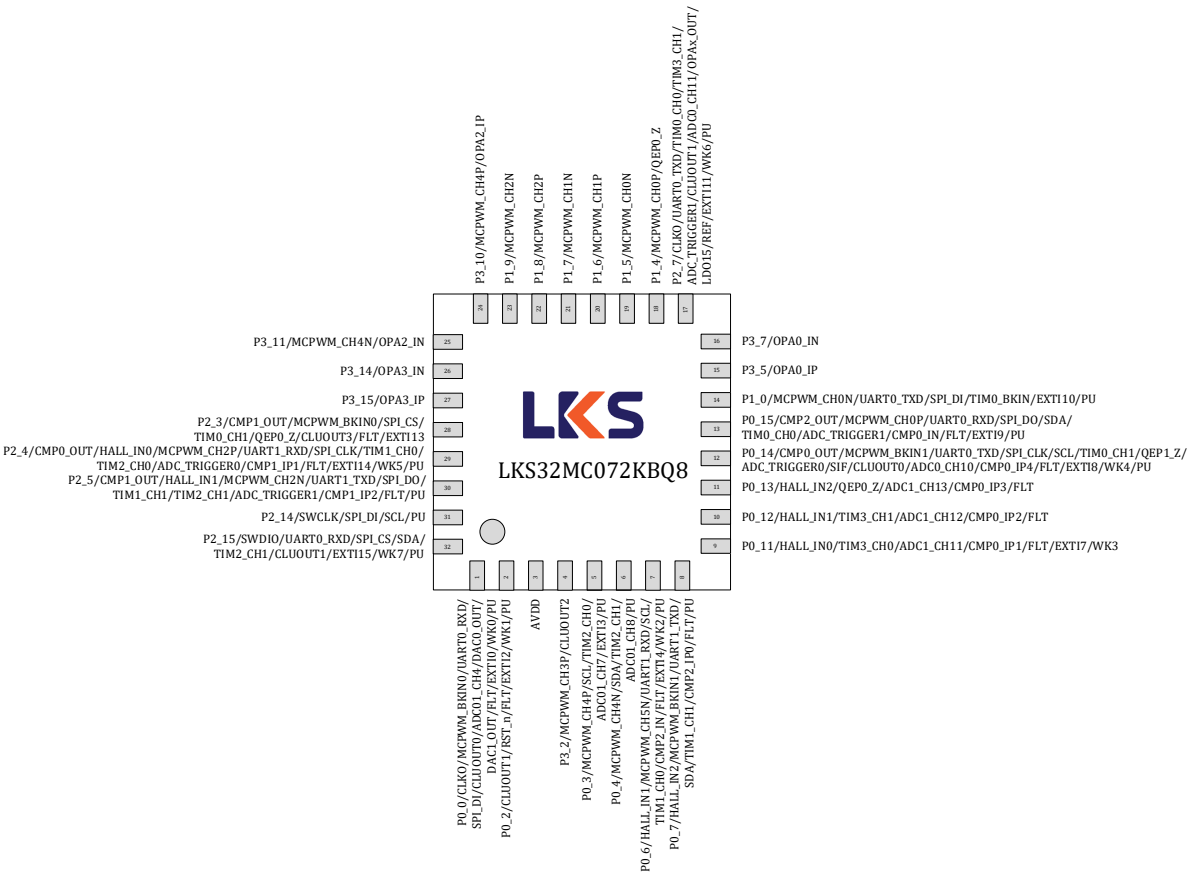



Fig.3-4 LKS32MC072KBQ8 Pin Assignment

* The red PIN pin in the figure has a built-in resistor that pulls up to AVDD:
The RSTN has an internal 300 kΩ pull-up resistor and is fixed on pull-up
SWDIO/SWCLK has a 12kΩ internal pull-up resistor and is fixed on pull-up.
The remaining red PIN pins have built-in 12 kΩ pull-up resistors, which can be turned on and off by software control.

Table 3-4 LKS32MC072KBQ8 Pin Function Description

| | | |
|---|---|---|
| 0 | GND | In the heat dissipation area of the abdomen, Pad is the chip GND |
| 1 | P0_0 | P0.0 |
| | CLKO | Clock output (for debugging) |
| | MCPWM_BKIN0 | PWM shutdown input signal 0 |
| | UART0_RXD | Serial port 0 receive (send) |
| | SPI_DI | SPI Data In (Out) |
| | CLUOUT0 | CLU0 output |
| | ADC01_CH4 | ADC 0/ADC1 Channel 4 |
| | DAC0_OUT | DAC0 output |
| | DAC1_OUT | DAC1 Output |
| | FLT | IO filtering |

| | | |
|---|---|---|
| | EXTI0 | External GPIO Interrupt Signal 0 |
| | WK0 | External wake-up signal 0 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 2 | P0_2 | P0.2 |
| | CLUOUT1 | CLU1 output |
| | RST_n | Reset pin, P0.2 used as RSTN by default. It is recommended to connect a 10 nF to 100 nF capacitor to ground and place a 12 K to 20 K pull-up resistor between RSTN and AVDD. If there is an external pull-up resistor, the capacitance of RSTN should be 100 nF. P0.2 can be switched as a GPIO, which turns off the 12 kΩ pull-up resistor. |
| | FLT | IO filtering |
| | EXTI2 | External GPIO Interrupt Signal 2 |
| | WK1 | External wake-up signal 1 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 3 | AVDD | Chip power supply, power supply range 2.5 ~ 5.5V |
| 4 | P3_2 | P3.2 |
| | MCPWM_CH3P | PWM Channel 3 High-Side |
| | CLUOUT2 | CLU2 output |
| 5 | P0_3 | P0.3 |
| | MCPWM_CH4P | PWM Channel 4 High Side |
| | SCL | I2C clock |
| | TIM2_CH0 | Timer2 channel 0 |
| | ADC01_CH7 | ADC0/ADC1 Channel 7 |
| | EXTI3 | External GPIO Interrupt Signal 3 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 6 | P0_4 | P0.4 |
| | MCPWM_CH4N | PWM Channel 4 Low Side |
| | SDA | I2C data |
| | TIM2_CH1 | Timer2 channel 1 |
| | ADC01_CH8 | ADC0/ADC1 Channel 8 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 7 | P0_6 | P0.6 |
| | HALL_IN1 | HALL interface input 1 |
| | MCPWM_CH5N | PWM Channel 5 Low Side |
| | UART1_RXD | Serial port 1 receive (send) |
| | SCL | I2C clock |
| | TIM1_CH0 | Timer1 channel 0 |
| | CMP2_IN | Comparator 2 Negative Terminal Input |
| | FLT | IO filtering |
| | EXTI4 | External GPIO Interrupt 4 |
| | WK2 | External wake-up signal 2 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 8 | P0_7 | P0.7 |

| | | |
|---|---|---|
| | HALL_IN2 | HALL interface input 2 |
| | MCPWM_BKIN1 | PWM Shutdown Input Signal 1 |
| | UART1_TXD | Serial port 1 send (receive) |
| | SDA | I2C data |
| | TIM1_CH1 | Timer1 channel 1 |
| | CMP2_IP0 | Positive input 0 of comparator 2 |
| | FLT | IO filtering |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 9 | P0_11 | P0.11 |
| | HALL_IN0 | HALL interface input 0 |
| | TIM3_CH0 | Timer3 channel 0 |
| | ADC1_CH11 | ADC1 Channel 11 |
| | CMP0_IP1 | Comparator 0 positive input 1 |
| | FLT | IO filtering |
| | EXTI7 | External GPIO Interrupt Signal 7 |
| | WK3 | External wake-up signal 3 |
| 10 | P0_12 | P0.12 |
| | HALL_IN1 | HALL interface input 1 |
| | TIM3_CH1 | Timer3 channel 1 |
| | ADC1_CH12 | ADC1 Channel 12 |
| | CMP0_IP2 | Comparator 0 positive input 2 |
| | FLT | IO filtering |
| 11 | P0_13 | P0.13 |
| | HALL_IN2 | HALL interface input 2 |
| | QEP0_Z | QEP0 Encoder Phase Z |
| | ADC1_CH13 | ADC1 Channel 13 |
| | CMP0_IP3 | Comparator 0 positive input 3 |
| | FLT | IO filtering |
| 12 | P0_14 | P0.14 |
| | CMP0_OUT | Comparator 0 Output |
| | MCPWM_BKIN1 | PWM Shutdown Input Signal 1 |
| | UART0_TXD | Serial port 0 send (receive) |
| | SPI_CLK | SPI clock |
| | SCL | I2C clock |
| | TIM0_CH1 | Timer0 channel 1 |
| | QEP1_Z | Phase Z of QEP1 encoder |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | SIF | Single line communication |
| | CLUOUT0 | CLU0 output |
| | ADC0_CH10 | ADC0 Channel 10 |
| | CMP0_IP4 | Comparator 0 positive input 4 |
| | FLT | IO filtering |
| | EXTI8 | External GPIO Interrupt Signal 8 |

| | | |
|---|---|---|
| | WK4 | External wake-up signal 4 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 13 | P0_15 | P0.15 |
| | CMP2_OUT | Comparator 2 Output |
| | MCPWM_CH0P | PWM Channel 0 High Side |
| | UART0_RXD | Serial port 0 receive (send) |
| | SPI_DO | SPI Data Output (Input) |
| | SDA | I2C data |
| | TIM0_CH0 | Timer0 channel 0 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | CMP0_IN | Comparator 0 negative input |
| | FLT | IO filtering |
| | EXTI9 | External GPIO Interrupt 9 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 14 | P1_0 | P1.0 |
| | MCPWM_CH0N | PWM Channel 0 Low Side |
| | UART0_TXD | Serial port 0 send (receive) |
| | SPI_DI | SPI Data In (Out) |
| | TIM0_BKIN | TIMER0 _ FAIL signal from GPIO |
| | EXTI10 | External GPIO Interrupt Signal 10 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 15 | P3_5 | P3.5 |
| | OPA0_IP | Positive terminal input of operational amplifier 0 |
| 16 | P3_7 | P3.7 |
| | OPA0_IN | Input of negative terminal of operational amplifier 0 |
| 17 | P2_7 | P2.7 |
| | CLKO | Clock output (for debugging) |
| | UART0_TXD | Serial port 0 send (receive) |
| | TIM0_CH0 | Timer0 channel 0 |
| | TIM3_CH1 | Timer3 channel 1 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | CLUOUT1 | CLU1 output |
| | ADC0_CH11 | ADC0 Channel 11 |
| | OPAx_OUT | Op Amp Output |
| | LDO15 | 1.5V LDO Output |
| | REF | Reference Voltage |
| | EXTI11 | External GPIO Interrupt Signal 11 |
| | WK6 | External wake-up signal 6 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 18 | P1_4 | P1.4 |
| | MCPWM_CH0P | PWM Channel 0 High Side |
| | QEP0_Z | QEP0 Encoder Phase Z |
| 19 | P1_5 | P1.5 |

| | | |
|---|---|---|
| | MCPWM_CH0N | PWM Channel 0 Low Side |
| 20 | P1_6 | P1.6 |
| | MCPWM_CH1P | PWM Channel 1 High Side |
| 21 | P1_7 | P1.7 |
| | MCPWM_CH1N | PWM Channel 1 Low Side |
| 22 | P1_8 | P1.8 |
| | MCPWM_CH2P | PWM Channel 2 High Side |
| 23 | P1_9 | P1.9 |
| | MCPWM_CH2N | PWM Channel 2 Low Side |
| 24 | P3_10 | P3.10 |
| | MCPWM_CH4P | PWM Channel 4 High Side |
| | OPA2_IP | Positive input of operational amplifier 2 |
| 25 | P3_11 | P3.11 |
| | MCPWM_CH4N | PWM Channel 4 Low Side |
| | OPA2_IN | Op Amp 2 Negative Input |
| 26 | P3_14 | P3.14 |
| | OPA3_IN | Op Amp 3 Negative Input |
| 27 | P3_15 | P3.15 |
| | OPA3_IP | Positive input of operational amplifier 3 |
| 28 | P2_3 | P2.3 |
| | CMP1_OUT | Comparator 1 Output |
| | MCPWM_BKIN0 | PWM shutdown input signal 0 |
| | SPI_CS | SPI chip select |
| | TIM0_CH1 | Timer0 channel 1 |
| | QEP0_Z | QEP0 Encoder Phase Z |
| | CLUOUT3 | CLU3 output |
| | FLT | IO filtering |
| | EXTI13 | External GPIO Interrupt Signal 13 |
| 29 | P2_4 | P2.4 |
| | CMP0_OUT | Comparator 0 Output |
| | HALL_IN0 | HALL interface input 0 |
| | MCPWM_CH2P | PWM Channel 2 High Side |
| | UART1_RXD | Serial port 1 receive (send) |
| | SPI_CLK | SPI clock |
| | TIM1_CH0 | Timer1 channel 0 |
| | TIM2_CH0 | Timer2 channel 0 |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | CMP1_IP1 | Comparator 1 positive input 1 |
| | FLT | IO filtering |
| | EXTI14 | External GPIO Interrupt Signal 14 |
| | WK5 | External wake-up signal 5 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 30 | P2_5 | P2.5 |

| | | |
|---|---|---|
| | CMP1_OUT | Comparator 1 Output |
| | HALL_IN1 | HALL interface input 1 |
| | MCPWM_CH2N | PWM Channel 2 Low Side |
| | UART1_TXD | Serial port 1 send (receive) |
| | SPI_DO | SPI Data Output (Input) |
| | TIM1_CH1 | Timer1 channel 1 |
| | TIM2_CH1 | Timer2 channel 1 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | CMP1_IP2 | Comparator 1 positive input 2 |
| | FLT | IO filtering |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 31 | P2_14 | P2.14 |
| | SWCLK | SWD clock |
| | SPI_DI | SPI Data In (Out) |
| | SCL | I2C clock |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 32 | P2_15 | P2.15 |
| | SWDIO | SWD data |
| | UART0_RXD | Serial port 0 receive (send) |
| | SPI_CS | SPI chip select |
| | SDA | I2C data |
| | TIM2_CH1 | Timer2 channel 1 |
| | CLUOUT1 | CLU1 output |
| | EXTI15 | External GPIO Interrupt 15 |
| | WK7 | External wake-up signal 7 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |

### 3.1.5 LKS32MC072KBT8

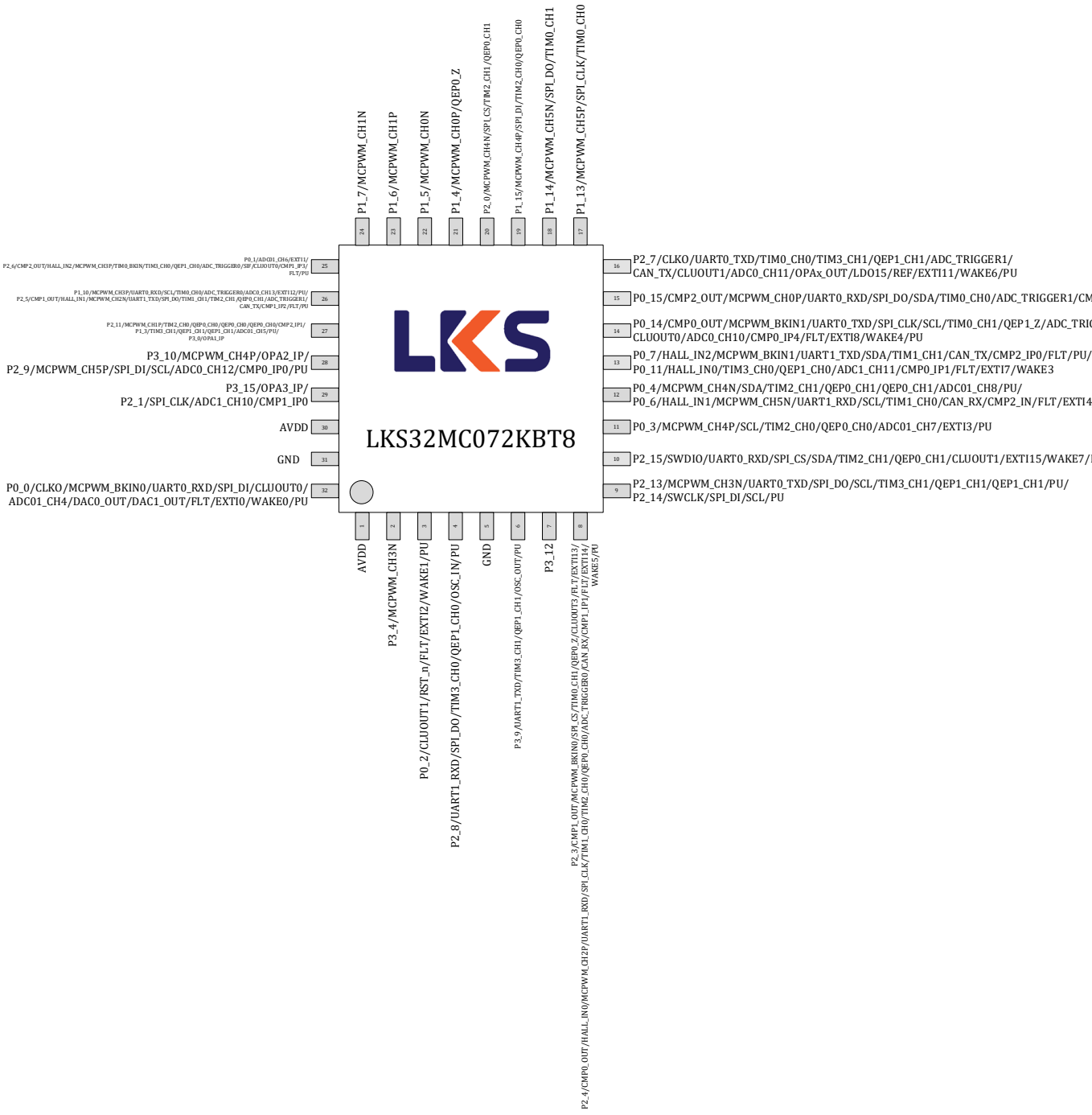



Fig.3-5 LKS32MC072KBT8 Pin Assignment

Note:

To be compatible with RX13T, the MCPWM output sequence and GPIO corresponding sequence of 072KBT8 are different from other 07x series MCU. Need to configure PWM SWAP=2 to account for

this difference.

Table 3-5 LKS32MC072KBT8 Pin Function Description

| | | |
|---|---|---|
| 1 | AVDD | Chip power supply, power supply range 2.5 ~ 5.5V |
| 2 | P3_4 | P3.4 |
| | MCPWM_CH3N | PWM channel 3 low-side |
| 3 | P0_2 | P0.2 |
| | CLUOUT1 | CLU1 output |
| | RST_n | P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 12k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 12kΩ pull-up resistor could be turned-off by software. |
| | FLT | IO filter |
| | EXTI2 | External GPIO interrupt input signal 2 |
| | WAKE1 | External wake-up signal 1 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 4 | P2_8 | P2.8 |
| | UART1_RXD | UART1 receive(transmit) |
| | SPI_DO | SPI data output(input) |
| | TIM3_CH0 | Timer3 channel0 |
| | QEP1_CH0 | Encoder1 channel0 |
| | OSC_IN | External crystal oscillator pin |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 5 | GND | GND |
| 6 | P3_9 | P3.9 |
| | UART1_TXD | UART1 transmit(receive) |
| | TIM3_CH1 | Timer3 channel1 |
| | QEP1_CH1 | Encoder1 channel1 |
| | OSC_OUT | External crystal oscillator pin |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 7 | P3_12 | P3.12 |
| 8 | P2_3 | P2.3 |
| | CMP1_OUT | Comparator 1 output |
| | MCPWM_BKIN0 | PWM break signal 0 |
| | SPI_CS | SPI chip select |
| | TIM0_CH1 | Timer0 channel1 |
| | QEP0_Z | QEP0 encoder Z phase |
| | CLUOUT3 | CLU3 output |
| | FLT | IO filter |
| | EXTI13 | External GPIO interrupt input signal 13 |
| | P2_4 | P2.4 |
| | CMP0_OUT | Comparator 0 output |

| | | |
|---|---|---|
| | HALL_IN0 | Hall interface input 0 |
| | MCPWM_CH5N | PWM channel 5 low-side |
| | UART1_RXD | UART1 receive(transmit) |
| | SPI_CLK | SPI clock |
| | TIM1_CH0 | Timer1 channel0 |
| | TIM2_CH0 | Timer2 channel0 |
| | QEP0_CH0 | Encoder0 channel0 |
| | ADC_TRIGGER0 | ADC0 trigger for debug |
| | CAN_RX | CAN Receive |
| | CMP1_IP1 | Comparator1 positive input1 |
| | FLT | IO filter |
| | EXTI14 | External GPIO interrupt input signal 14 |
| | WAKE5 | External wake-up signal 5 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 9 | P2_13 | P2.13 |
| | MCPWM_CH5P | PWM channel 5 high-side |
| | UART0_TXD | UART0 transmit(receive) |
| | SPI_DO | SPI data output(input) |
| | SCL | I2C clock |
| | TIM3_CH1 | Timer3 channel1 |
| | QEP1_CH1 | Encoder1 channel1 |
| | QEP1_CH1 | Encoder1 channel1 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| | P2_14 | P2.14 |
| | SWCLK | SWD Clock |
| | SPI_DI | SPI data input(output) |
| | SCL | I2C clock |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 10 | P2_15 | P2.15 |
| | SWDIO | SWD Data |
| | UART0_RXD | UART0 receive(transmit) |
| | SPI_CS | SPI chip select |
| | SDA | I2C data |
| | TIM2_CH1 | Timer2 channel1 |
| | QEP0_CH1 | Encoder0 channel1 |
| | CLUOUT1 | CLU1 output |
| | EXTI15 | External GPIO interrupt input signal 15 |
| | WAKE7 | External wake-up signal 7 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 11 | P0_3 | P0.3 |
| | MCPWM_CH2N | PWM channel 2 low-side |
| | SCL | I2C clock |
| | TIM2_CH0 | Timer2 channel0 |

| | | |
|---|---|---|
| | QEP0_CH0 | Encoder0 channel0 |
| | ADC01_CH7 | ADC01 channel 7 |
| | EXTI3 | External GPIO interrupt input signal 3 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 12 | P0_4 | P0.4 |
| | MCPWM_CH0P | PWM channel 0 high-side |
| | SDA | I2C data |
| | TIM2_CH1 | Timer2 channel1 |
| | QEP0_CH1 | Encoder0 channel1 |
| | QEP0_CH1 | Encoder0 channel1 |
| | ADC01_CH8 | ADC01 channel 8 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| | P0_6 | P0.6 |
| | HALL_IN1 | Hall interface input 1 |
| | MCPWM_CH1N | PWM channel 1 low-side |
| | UART1_RXD | UART1 receive(transmit) |
| | SCL | I2C clock |
| | TIM1_CH0 | Timer1 channel0 |
| | CAN_RX | CAN Receive |
| | CMP2_IN | Comparator2 negative input |
| | FLT | IO filter |
| | EXTI4 | External GPIO interrupt input signal 4 |
| | WAKE2 | External wake-up signal 2 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 13 | P0_7 | P0.7 |
| | HALL_IN2 | Hall interface input 2 |
| | MCPWM_BKIN1 | PWM break signal 1 |
| | UART1_TXD | UART1 transmit(receive) |
| | SDA | I2C data |
| | TIM1_CH1 | Timer1 channel1 |
| | CAN_TX | CAN Transmit |
| | CMP2_IP0 | Comparator2 positive input0 |
| | FLT | IO filter |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| | P0_11 | P0.11 |
| | HALL_IN0 | Hall interface input 0 |
| | TIM3_CH0 | Timer3 channel0 |
| | QEP1_CH0 | Encoder1 channel0 |
| | ADC1_CH11 | ADC1 channel 11 |
| | CMP0_IP1 | Comparator0 positive input1 |
| | FLT | IO filter |
| | EXTI7 | External GPIO interrupt input signal 7 |
| | WAKE3 | External wake-up signal 3 |

| | | |
|---|---|---|
| 14 | P0_14 | P0.14 |
| | CMP0_OUT | Comparator 0 output |
| | MCPWM_BKIN1 | PWM break signal 1 |
| | UART0_TXD | UART0 transmit(receive) |
| | SPI_CLK | SPI clock |
| | SCL | I2C clock |
| | TIM0_CH1 | Timer0 channel1 |
| | QEP1_Z | QEP1 encoder Z phase |
| | ADC_TRIGGER0 | ADC0 trigger for debug |
| | SIF | Single line communication |
| | CLUOUT0 | CLU0 output |
| | ADC0_CH10 | ADC0 channel 10 |
| | CMP0_IP4 | Comparator0 positive input4 |
| | FLT | IO filter |
| | EXTI8 | External GPIO interrupt input signal 8 |
| | WAKE4 | External wake-up signal 4 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 15 | P0_15 | P0.15 |
| | CMP2_OUT | Comparator 2 output |
| | MCPWM_CH1P | PWM channel 1 high-side |
| | UART0_RXD | UART0 receive(transmit) |
| | SPI_DO | SPI data output(input) |
| | SDA | I2C data |
| | TIM0_CH0 | Timer0 channel0 |
| | ADC_TRIGGER1 | ADC1 trigger for debug |
| | CMP0_IN | Comparator0 negative input |
| | FLT | IO filter |
| | EXTI9 | External GPIO interrupt input signal 9 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 16 | P2_7 | P2.7 |
| | CLKO | Clock output for debug |
| | UART0_TXD | UART0 transmit(receive) |
| | TIM0_CH0 | Timer0 channel0 |
| | TIM3_CH1 | Timer3 channel1 |
| | QEP1_CH1 | Encoder1 channel1 |
| | ADC_TRIGGER1 | ADC1 trigger for debug |
| | CAN_TX | CAN Transmit |
| | CLUOUT1 | CLU1 output |
| | ADC0_CH11 | ADC0 channel 11 |
| | OPAx_OUT | OPA output |
| | LDO15 | 1.5V LDO output |
| | REF | Reference voltage output for debug |
| | EXTI11 | External GPIO interrupt input signal 11 |

| | | |
|---|---|---|
| | WAKE6 | External wake-up signal 6 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 17 | P1_13 | P1.13 |
| | MCPWM_CH0N | PWM channel 0 low-side |
| | SPI_CLK | SPI clock |
| | TIM0_CH0 | Timer0 channel0 |
| 18 | P1_14 | P1.14 |
| | MCPWM_CH1N | PWM channel 1 low-side |
| | SPI_DO | SPI data output(input) |
| | TIM0_CH1 | Timer0 channel1 |
| 19 | P1_15 | P1.15 |
| | MCPWM_CH2N | PWM channel 2 low-side |
| | SPI_DI | SPI data input(output) |
| | TIM2_CH0 | Timer2 channel0 |
| | QEP0_CH0 | Encoder0 channel0 |
| 20 | P2_0 | P2.0 |
| | MCPWM_CH0P | PWM channel 0 high-side |
| | SPI_CS | SPI chip select |
| | TIM2_CH1 | Timer2 channel1 |
| | QEP0_CH1 | Encoder0 channel1 |
| 21 | P1_4 | P1.4 |
| | MCPWM_CH1P | PWM channel 1 high-side |
| | QEP0_Z | QEP0 encoder Z phase |
| 22 | P1_5 | P1.5 |
| | MCPWM_CH2P | PWM channel 2 high-side |
| 23 | P1_6 | P1.6 |
| | MCPWM_CH3N | PWM channel 3 low-side |
| 24 | P1_7 | P1.7 |
| | MCPWM_CH4N | PWM channel 4 low-side |
| 25 | P0_1 | P0.1 |
| | ADC01_CH6 | PWM channel 5 low-side |
| | EXTI1 | External GPIO interrupt input signal 1 |
| | P2_6 | P2.6 |
| | CMP2_OUT | Comparator 2 Output |
| | HALL_IN2 | Hall interface input 2 |
| | MCPWM_CH3P | PWM channel 4 high-side |
| | TIM0_BKIN | TIMER0 _ FAIL signal from GPIO |
| | TIM3_CH0 | Timer3 channel0 |
| | QEP1_CH0 | Encoder1 channel0 |
| | ADC_TRIGGER0 | ADC0 trigger for debug |
| | SIF | Single line communication |
| | CLUOUT0 | CLU0 output |
| | CMP1_IP3 | Comparator 1 positive input 3 |

| | | |
|---|---|---|
| | FLT | IO filter |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 26 | P1_10 | P1.10 |
| | MCPWM_CH3P | PWM channel 4 high-side |
| | UART0_RXD | UART0 receive(transmit) |
| | SCL | I2C clock |
| | TIM0_CH0 | Timer0 channel0 |
| | ADC_TRIGGER0 | ADC0 trigger for debug |
| | ADC0_CH13 | ADC0 channel 13 |
| | EXTI12 | External GPIO interrupt input signal 12 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 10 | P2_5 | P2.5 |
| | CMP1_OUT | Comparator 1 Output |
| | HALL_IN1 | Hall interface input 1 |
| | MCPWM_CH2N | PWM channel 2 low-side |
| | UART1_TXD | UART1 transmit(receive) |
| | SPI_DO | SPI Data Output (Input) |
| | TIM1_CH1 | Timer1 channel1 |
| | TIM2_CH1 | Timer2 channel1 |
| | QEP0_CH1 | Encoder0 channel1 |
| | ADC_TRIGGER1 | ADC1 trigger for debug |
| | CAN_TX | CAN Transmit |
| | CMP1_IP2 | Comparator 1 positive input 2 |
| | FLT | IO filter |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 27 | P3_0 | P3.0 |
| | OPA1_IP | OPA1 positive input |
| 28 | P3_10 | P3.10 |
| | MCPWM_CH2N | PWM channel 2 low-side |
| | OPA2_IP | OPA2 positive input |
| | P2_9 | P2.9 |
| | MCPWM_CH0N | PWM channel 0 low-side |
| | SPI_DI | SPI data input(output) |
| | SCL | I2C clock |
| | ADC0_CH12 | ADC0 channel 12 |
| | CMP0_IP0 | Comparator0 positive input0 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 29 | P3_15 | P3.15 |
| | OPA3_IP | OPA3 positive input |
| | P2_1 | P2.1 |
| | SPI_CLK | SPI clock |
| | ADC1_CH10 | ADC1 channel 10 |
| | CMP1_IP0 | Comparator1 positive input0 |

| | | |
|---|---|---|
| 30 | AVDD | Power supply, 2.2~5.5V |
| 31 | GND | Ground |
| 32 | P0_0 | P0.0 |
| | CLKO | Clock output for debug |
| | MCPWM_BKIN0 | PWM break signal 0 |
| | UART0_RXD | UART0 receive(transmit) |
| | SPI_DI | SPI data input(output) |
| | CLUOUT0 | CLU0 output |
| | ADC01_CH4 | ADC01 channel 4 |
| | DAC0_OUT | DAC0 out put |
| | DAC1_OUT | DAC1 out put |
| | FLT | IO filter |
| | EXTI0 | External GPIO interrupt input signal 0 |
| | WAKE0 | External wake-up signal 0 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |

### 3.1.6 LKS32MC073HBQ8

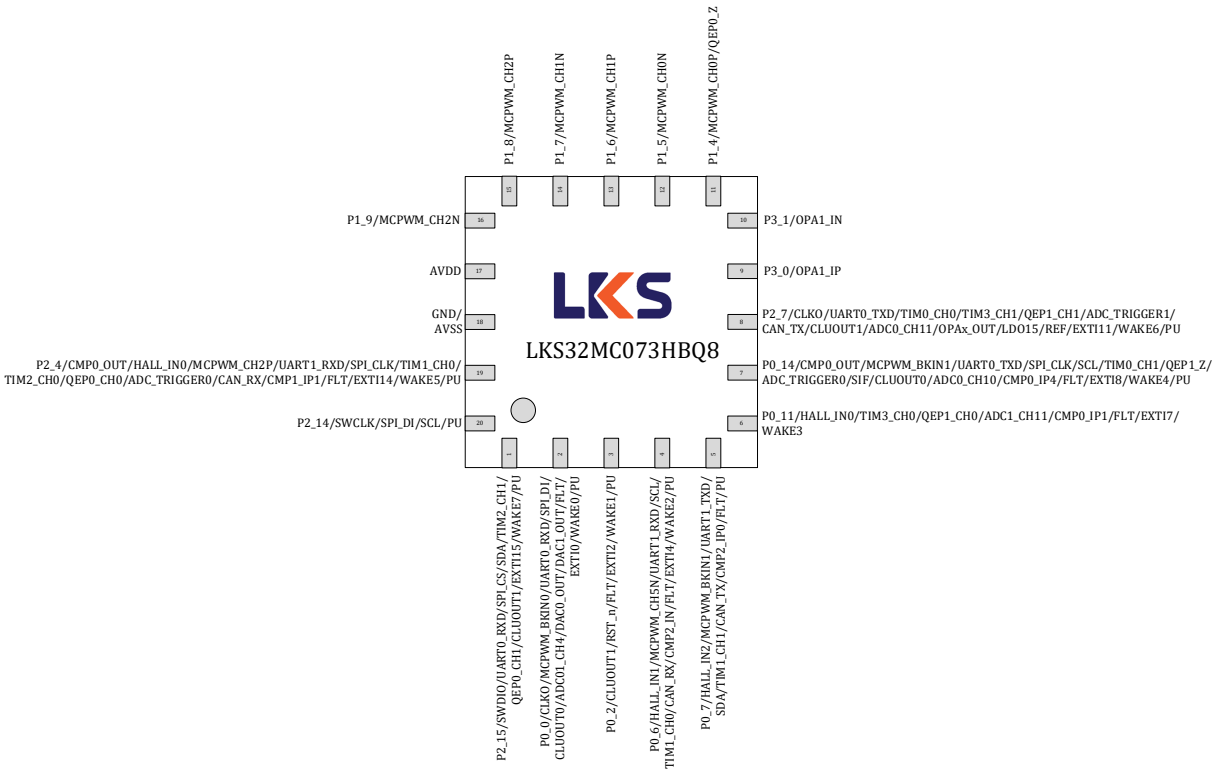



Fig.3-6 LKS32MC073HBQ8 Pin Assignment

The RSTN has an internal 300 kΩ pull-up resistor and is fixed on pull-up
SWDIO/SWCLK has a 12kΩ internal pull-up resistor and is fixed on pull-up.

Table 3-6 LKS32MC073HBQ8 Pin Function Description

| | | |
|---|---|---|
| 0 | GND | In the heat dissipation area of the abdomen, Pad is the chip GND |
| 1 | P2_15 | P2.15 |
| | SWDIO | SWD Data |
| | UART0_RXD | UART0 receive(transmit) |
| | SPI_CS | SPI chip select |
| | SDA | I2C data |
| | TIM2_CH1 | Timer2 channel1 |
| | QEP0_CH1 | Encoder0 channel1 |
| | CLUOUT1 | CLU1 output |
| | EXTI15 | External GPIO interrupt input signal 15 |
| | WAKE7 | External wake-up signal 7 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 2 | P0_0 | P0.0 |
| | CLKO | Clock output for debug |
| | MCPWM_BKIN0 | PWM break signal 0 |
| | UART0_RXD | UART0 receive(transmit) |
| | SPI_DI | SPI data input(output) |
| | CLUOUT0 | CLU0 output |
| | ADC01_CH4 | ADC01 channel 4 |
| | DAC0_OUT | DAC0 out put |
| | DAC1_OUT | DAC1 out put |
| | FLT | IO filter |
| | EXTI0 | External GPIO interrupt input signal 0 |
| | WAKE0 | External wake-up signal 0 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 3 | P0_2 | P0.2 |
| | CLUOUT1 | CLU1 output |
| | RST_n | P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 12k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 12kΩ pull-up resistor could be turned-off by software. |
| | FLT | IO filter |
| | EXTI2 | External GPIO interrupt input signal 2 |
| | WAKE1 | External wake-up signal 1 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 4 | P0_6 | P0.6 |
| | HALL_IN1 | Hall interface input 1 |
| | MCPWM_CH5N | PWM channel 5 low-side |
| | UART1_RXD | UART1 receive(transmit) |
| | SCL | I2C clock |
| | TIM1_CH0 | Timer1 channel0 |

| | | |
|---|---|---|
| | CAN_RX | CAN Receive |
| | CMP2_IN | Comparator2 negative input |
| | FLT | IO filter |
| | EXTI4 | External GPIO interrupt input signal 4 |
| | WAKE2 | External wake-up signal 2 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 5 | P0_7 | P0.7 |
| | HALL_IN2 | Hall interface input 2 |
| | MCPWM_BKIN1 | PWM break signal 1 |
| | UART1_TXD | UART1 transmit(receive) |
| | SDA | I2C data |
| | TIM1_CH1 | Timer1 channel1 |
| | CAN_TX | CAN Transmit |
| | CMP2_IP0 | Comparator2 positive input0 |
| | FLT | IO filter |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 6 | P0_11 | P0.11 |
| | HALL_IN0 | Hall interface input 0 |
| | TIM3_CH0 | Timer3 channel0 |
| | QEP1_CH0 | Encoder1 channel0 |
| | ADC1_CH11 | ADC1 channel 11 |
| | CMP0_IP1 | Comparator0 positive input1 |
| | FLT | IO filter |
| | EXTI7 | External GPIO interrupt input signal 7 |
| | WAKE3 | External wake-up signal 3 |
| 7 | P0_14 | P0.14 |
| | CMP0_OUT | Comparator 0 output |
| | MCPWM_BKIN1 | PWM break signal 1 |
| | UART0_TXD | UART0 transmit(receive) |
| | SPI_CLK | SPI clock |
| | SCL | I2C clock |
| | TIM0_CH1 | Timer0 channel1 |
| | QEP1_Z | QEP1 encoder Z phase |
| | ADC_TRIGGER0 | ADC0 trigger for debug |
| | SIF | Single line communication |
| | CLUOUT0 | CLU0 output |
| | ADC0_CH10 | ADC0 channel 10 |
| | CMP0_IP4 | Comparator0 positive input4 |
| | FLT | IO filter |
| | EXTI8 | External GPIO interrupt input signal 8 |
| | WAKE4 | External wake-up signal 4 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 8 | P2_7 | P2.7 |

| | | |
|---|---|---|
| | CLKO | Clock output for debug |
| | UART0_TXD | UART0 transmit(receive) |
| | TIM0_CH0 | Timer0 channel0 |
| | TIM3_CH1 | Timer3 channel1 |
| | QEP1_CH1 | Encoder1 channel1 |
| | ADC_TRIGGER1 | ADC1 trigger for debug |
| | CAN_TX | CAN Transmit |
| | CLUOUT1 | CLU1 output |
| | ADC0_CH11 | ADC0 channel 11 |
| | OPAx_OUT | OPA output |
| | LDO15 | 1.5V LDO output |
| | REF | Reference voltage output for debug |
| | EXTI11 | External GPIO interrupt input signal 11 |
| | WAKE6 | External wake-up signal 6 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 9 | P3_0 | P3.0 |
| | OPA1_IP | OPA1 positive input |
| 10 | P3_1 | P3.1 |
| | OPA1_IN | OPA1 negative input |
| 11 | P1_4 | P1.4 |
| | MCPWM_CH0P | PWM channel 0 high-side |
| | QEP0_Z | QEP0 encoder Z phase |
| 12 | P1_5 | P1.5 |
| | MCPWM_CH0N | PWM channel 0 low-side |
| 13 | P1_6 | P1.6 |
| | MCPWM_CH1P | PWM channel 1 high-side |
| 14 | P1_7 | P1.7 |
| | MCPWM_CH1N | PWM channel 1 low-side |
| 15 | P1_8 | P1.8 |
| | MCPWM_CH2P | PWM channel 2 high-side |
| 16 | P1_9 | P1.9 |
| | MCPWM_CH2N | PWM channel 2 low-side |
| 17 | AVDD | Power supply, 2.2~5.5V |
| 18 | GND | Ground |
| 19 | P2_4 | P2.4 |
| | CMP0_OUT | Comparator 0 output |
| | HALL_IN0 | Hall interface input 0 |
| | MCPWM_CH2P | PWM channel 2 high-side |
| | UART1_RXD | UART1 receive(transmit) |
| | SPI_CLK | SPI clock |
| | TIM1_CH0 | Timer1 channel0 |
| | TIM2_CH0 | Timer2 channel0 |
| | QEP0_CH0 | Encoder0 channel0 |

| | | |
|---|---|---|
| | ADC_TRIGGER0 | ADC0 trigger for debug |
| | CAN_RX | CAN Receive |
| | CMP1_IP1 | Comparator1 positive input1 |
| | FLT | IO filter |
| | EXTI14 | External GPIO interrupt input signal 14 |
| | WAKE5 | External wake-up signal 5 |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |
| 20 | P2_14 | P2.14 |
| | SWCLK | SWD Clock |
| | SPI_DI | SPI data input(output) |
| | SCL | I2C clock |
| | PU | Built-in 12kΩ Pull-up resistor which could be turn-off by software |

### 3.1.7 LKS32MC077MBS8

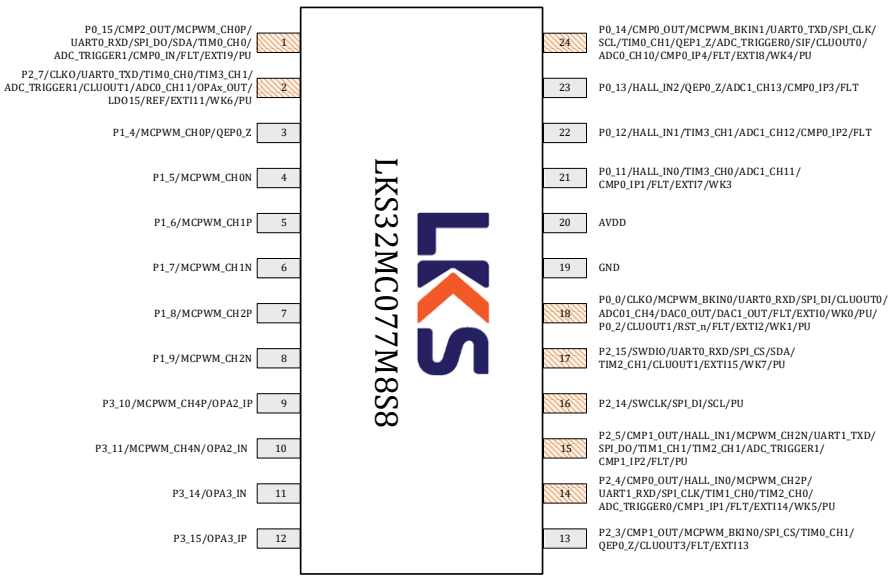



Fig.3-7 LKS32MC077MBS8 Pin Assignment

* The red PIN pin in the figure has a built-in resistor that pulls up to AVDD:
The RSTN has an internal 300 kΩ pull-up resistor and is fixed on pull-up
SWDIO/SWCLK has a 12kΩ internal pull-up resistor and is fixed on pull-up.
The remaining red PIN pins have built-in 12 kΩ pull-up resistors, which can be turned on and off by software control.

Table 3-7 LKS32MC077MBS8 Pin Function Description

| | | |
|---|---|---|
| 1 | P0_15 | P0.15 |
| | CMP2_OUT | Comparator 2 Output |
| | MCPWM_CH0P | PWM Channel 0 High Side |
| | UART0_RXD | Serial port 0 receive (send) |

| | | |
|---|---|---|
| | SPI_DO | SPI Data Output (Input) |
| | SDA | I2C data |
| | TIM0_CH0 | Timer0 channel 0 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | CMP0_IN | Comparator 0 negative input |
| | FLT | IO filtering |
| | EXTI9 | External GPIO Interrupt 9 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 2 | P2_7 | P2.7 |
| | CLKO | Clock output (for debugging) |
| | UART0_TXD | Serial port 0 send (receive) |
| | TIM0_CH0 | Timer0 channel 0 |
| | TIM3_CH1 | Timer3 channel 1 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | CLUOUT1 | CLU1 output |
| | ADC0_CH11 | ADC0 Channel 11 |
| | OPAx_OUT | Op Amp Output |
| | LDO15 | 1.5V LDO Output |
| | REF | Reference Voltage |
| | EXTI11 | External GPIO Interrupt Signal 11 |
| | WK6 | External wake-up signal 6 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 3 | P1_4 | P1.4 |
| | MCPWM_CH0P | PWM Channel 0 High Side |
| | QEP0_Z | QEP0 Encoder Phase Z |
| 4 | P1_5 | P1.5 |
| | MCPWM_CH0N | PWM Channel 0 Low Side |
| 5 | P1_6 | P1.6 |
| | MCPWM_CH1P | PWM Channel 1 High Side |
| 6 | P1_7 | P1.7 |
| | MCPWM_CH1N | PWM Channel 1 Low Side |
| 7 | P1_8 | P1.8 |
| | MCPWM_CH2P | PWM Channel 2 High Side |
| 8 | P1_9 | P1.9 |
| | MCPWM_CH2N | PWM Channel 2 Low Side |
| 9 | P3_10 | P3.10 |
| | MCPWM_CH4P | PWM Channel 4 High Side |
| | OPA2_IP | Positive input of operational amplifier 2 |
| 10 | P3_11 | P3.11 |
| | MCPWM_CH4N | PWM Channel 4 Low Side |
| | OPA2_IN | Op Amp 2 Negative Input |
| 11 | P3_14 | P3.14 |
| | OPA3_IN | Op Amp 3 Negative Input |

| | | |
|---|---|---|
| 12 | P3_15 | P3.15 |
| | OPA3_IP | Positive input of operational amplifier 3 |
| 13 | P2_3 | P2.3 |
| | CMP1_OUT | Comparator 1 Output |
| | MCPWM_BKIN0 | PWM shutdown input signal 0 |
| | SPI_CS | SPI chip select |
| | TIM0_CH1 | Timer0 channel 1 |
| | QEP0_Z | QEP0 Encoder Phase Z |
| | CLUOUT3 | CLU3 output |
| | FLT | IO filtering |
| | EXTI13 | External GPIO Interrupt Signal 13 |
| 14 | P2_4 | P2.4 |
| | CMP0_OUT | Comparator 0 Output |
| | HALL_IN0 | HALL interface input 0 |
| | MCPWM_CH2P | PWM Channel 2 High Side |
| | UART1_RXD | Serial port 1 receive (send) |
| | SPI_CLK | SPI clock |
| | TIM1_CH0 | Timer1 channel 0 |
| | TIM2_CH0 | Timer2 channel 0 |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | CMP1_IP1 | Comparator 1 positive input 1 |
| | FLT | IO filtering |
| | EXTI14 | External GPIO Interrupt Signal 14 |
| | WK5 | External wake-up signal 5 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 15 | P2_5 | P2.5 |
| | CMP1_OUT | Comparator 1 Output |
| | HALL_IN1 | HALL interface input 1 |
| | MCPWM_CH2N | PWM Channel 2 Low Side |
| | UART1_TXD | Serial port 1 send (receive) |
| | SPI_DO | SPI Data Output (Input) |
| | TIM1_CH1 | Timer1 channel 1 |
| | TIM2_CH1 | Timer2 channel 1 |
| | ADC_TRIGGER1 | ADC1 trigger signal output (for debugging) |
| | CMP1_IP2 | Comparator 1 positive input 2 |
| | FLT | IO filtering |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 16 | P2_14 | P2.14 |
| | SWCLK | SWD clock |
| | SPI_DI | SPI Data In (Out) |
| | SCL | I2C clock |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 17 | P2_15 | P2.15 |

| | | |
|---|---|---|
| | SWDIO | SWD data |
| | UART0_RXD | Serial port 0 receive (send) |
| | SPI_CS | SPI chip select |
| | SDA | I2C data |
| | TIM2_CH1 | Timer2 channel 1 |
| | CLUOUT1 | CLU1 output |
| | EXTI15 | External GPIO Interrupt 15 |
| | WK7 | External wake-up signal 7 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 18 | P0_2 | P0.2 |
| | CLUOUT1 | CLU1 output |
| | RST_n | Reset pin, P0.2 used as RSTN by default. It is recommended to connect a 10 nF to 100 nF capacitor to ground and place a 12 K to 20 K pull-up resistor between RSTN and AVDD. If there is an external pull-up resistor, the capacitance of RSTN should be 100 nF. P0.2 can be switched as a GPIO, which turns off the 12 kΩ pull-up resistor. |
| | FLT | IO filtering |
| | EXTI2 | External GPIO Interrupt Signal 2 |
| | WK1 | External wake-up signal 1 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |
| 19 | GND | Chip ground. It is strongly recommended that multiple ground pins be grounded uniformly on the PCB. |
| 20 | AVDD | Chip power supply, power supply range 2.5 ~ 5.5V |
| 21 | P0_11 | P0.11 |
| | HALL_IN0 | HALL interface input 0 |
| | TIM3_CH0 | Timer3 channel 0 |
| | ADC1_CH11 | ADC1 Channel 11 |
| | CMP0_IP1 | Comparator 0 positive input 1 |
| | FLT | IO filtering |
| | EXTI7 | External GPIO Interrupt Signal 7 |
| | WK3 | External wake-up signal 3 |
| 22 | P0_12 | P0.12 |
| | HALL_IN1 | HALL interface input 1 |
| | TIM3_CH1 | Timer3 channel 1 |
| | ADC1_CH12 | ADC1 Channel 12 |
| | CMP0_IP2 | Comparator 0 positive input 2 |
| | FLT | IO filtering |
| 23 | P0_13 | P0.13 |
| | HALL_IN2 | HALL interface input 2 |
| | QEP0_Z | QEP0 Encoder Phase Z |
| | ADC1_CH13 | ADC1 Channel 13 |
| | CMP0_IP3 | Comparator 0 positive input 3 |
| | FLT | IO filtering |
| 24 | P0_14 | P0.14 |

| | | |
|---|---|---|
| | CMP0_OUT | Comparator 0 Output |
| | MCPWM_BKIN1 | PWM Shutdown Input Signal 1 |
| | UART0_TXD | Serial port 0 send (receive) |
| | SPI_CLK | SPI clock |
| | SCL | I2C clock |
| | TIM0_CH1 | Timer0 channel 1 |
| | QEP1_Z | Phase Z of QEP1 encoder |
| | ADC_TRIGGER0 | ADC0 trigger signal output (for debugging) |
| | SIF | Single line communication |
| | CLUOUT0 | CLU0 output |
| | ADC0_CH10 | ADC0 Channel 10 |
| | CMP0_IP4 | Comparator 0 positive input 4 |
| | FLT | IO filtering |
| | EXTI8 | External GPIO Interrupt Signal 8 |
| | WK4 | External wake-up signal 4 |
| | PU | Built-in 12kΩ pull-up resistor, software switchable |

## 3.2 Description of Pin Multiplex Function

Table 3-8 LKS32MC07X Pin Function Selection

| Port | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P0.0 | CLKO | | MCPWM_BKIN0 | UART0_RXD | SPI_DI | | | | | | | CLUOUT0 | ADC01_CH4/ DAC0_OUT/ DAC1_OUT |
| P0.1 | | | | | | | | | | | | | ADC01_CH6 |
| P0.2 | | | | | | | | | | | | CLUOUT1 | |
| P0.3 | | | MCPWM_CH4P | | | SCL | | TIM2_CH0 | | | | | ADC01_CH7 |
| P0.4 | | | MCPWM_CH4N | | | SDA | | TIM2_CH1 | | | | | ADC01_CH8 |
| P0.5 | | HALL_IN0 | MCPWM_CH5P | | | | | QEP0_Z | | | | | ADC01_CH9 |
| P0.6 | | HALL_IN1 | MCPWM_CH5N | UART1_RXD | | SCL | TIM1_CH0 | | | CAN_RX | | | CMP2_IN |
| P0.7 | | HALL_IN2 | MCPWM_BKIN1 | UART1_TXD | | SDA | TIM1_CH1 | | | CAN_TX | | | CMP2_IP0 |
| P0.8 | | | | | | | | | | | | | |
| P0.9 | | | | | | SCL | | TIM2_CH0 | | | | | |
| P0.10 | | | | | | SDA | | TIM2_CH1 | | | | | |
| P0.11 | | HALL_IN0 | | | | | | TIM3_CH0 | | | | | ADC1_CH11/ CMP0_IP1 |
| P0.12 | | HALL_IN1 | | | | | | TIM3_CH1 | | CAN_RX | | | ADC1_CH12/ CMP0_IP2 |
| P0.13 | | HALL_IN2 | | | | | | QEP0_Z | | CAN_TX | | | ADC1_CH13/ CMP0_IP3 |
| P0.14 | CMP0_OUT | | MCPWM_BKIN1 | UART0_TXD | SPI_CLK | SCL | TIM0_CH1 | QEP1_Z | ADC_TRIGGER0 | | SIF | CLUOUT0 | ADC0_CH10/ CMP0_IP4 |
| P0.15 | CMP2_OUT | | MCPWM_CH0P | UART0_RXD | SPI_DO | SDA | TIM0_CH0 | | ADC_TRIGGER1 | | | | CMP0_IN |

Table 3-9 LKS32MC07X Pin Function Selection (continued)

| Port | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P1.0 | | | MCPWM_CH0N | UART0_TXD | SPI_DI | | TIM0_BKIN | | | | | | |
| P1.1 | | | | | SPI_CS | | | | | | | | |
| P1.2 | | | | | | | | TIM3_CH0 | | | | | |
| P1.3 | | | | | | | | TIM3_CH1 | | | | | ADC01_CH5 |
| P1.4 | | | MCPWM_CH0P | | | | | QEP0_Z | | | | | |
| P1.5 | | | MCPWM_CH0N | | | | | | | | | | |
| P1.6 | | | MCPWM_CH1P | | | | | | | | | | |
| P1.7 | | | MCPWM_CH1N | | | | | | | | | | |
| P1.8 | | | MCPWM_CH2P | | | | | | | | | | |
| P1.9 | | | MCPWM_CH2N | | | | | | | | | | |
| P1.10 | | | MCPWM_CH3P | UART0_RXD | | SCL | TIM0_CH0 | | ADC_TRIGGER0 | | | | ADC0_CH13 |
| P1.11 | | | MCPWM_CH3N | UART0_TXD | | SDA | TIM0_CH1 | | ADC_TRIGGER1 | | SIF | CLUOUT2 | |
| P1.12 | | | | | | | | | | | | | |
| P1.13 | | | MCPWM_CH5P | | SPI_CLK | | TIM0_CH0 | | | | | | |
| P1.14 | | | MCPWM_CH5N | | SPI_DO | | TIM0_CH1 | | | | | | |
| P1.15 | | | MCPWM_CH4P | | SPI_DI | | | TIM2_CH0 | | | | | |

Table 3-10 LKS32MC07X Pin Function Selection (continued)

| Port | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P2.0 | | | MCPWM_CH4N | | SPI_CS | | | TIM2_CH1 | | | | | |
| P2.1 | | | | | SPI_CLK | | | | | | | | ADC1_CH10/ CMP1_IP0 |
| P2.2 | | | | | | | | QEP1_Z | | | | | CMP1_IN |
| P2.3 | CMP1_OUT | | MCPWM_BKIN0 | | SPI_CS | | TIM0_CH1 | QEP0_Z | | | | CLUOUT3 | |
| P2.4 | CMP0_OUT | HALL_IN0 | MCPWM_CH2P | UART1_RXD | SPI_CLK | | TIM1_CH0 | TIM2_CH0 | ADC_TRIGGER0 | CAN_RX | | | CMP1_IP1 |
| P2.5 | CMP1_OUT | HALL_IN1 | MCPWM_CH2N | UART1_TXD | SPI_DO | | TIM1_CH1 | TIM2_CH1 | ADC_TRIGGER1 | CAN_TX | | | CMP1_IP2 |
| P2.6 | CMP2_OUT | HALL_IN2 | MCPWM_CH3P | | | | TIM0_BKIN | TIM3_CH0 | ADC_TRIGGER0 | | SIF | CLUOUT0 | CMP1_IP3 |
| P2.7 | CLKO | | | UART0_TXD | | | TIM0_CH0 | TIM3_CH1 | ADC_TRIGGER1 | CAN_TX | | CLUOUT1 | ADC0_CH11/ OPAx_OUT/ LDO15/REF |
| P2.8 | | | | UART1_RXD | SPI_DO | | | TIM3_CH0 | | | | | OSC_IN |
| P2.9 | | | MCPWM_CH5P | | SPI_DI | SCL | | | | | | | ADC0_CH12/ CMP0_IP0 |
| P2.10 | | | MCPWM_CH5N | | SPI_DO | SDA | | | | | | | |
| P2.11 | | | MCPWM_CH1P | | | | | TIM2_CH0 | | | | | CMP2_IP1 |
| P2.12 | | | MCPWM_CH1N | | SPI_CS | | | TIM2_CH1 | ADC_TRIGGER0 | | | CLUOUT3 | |
| P2.13 | | | MCPWM_CH3N | UART0_TXD | SPI_DO | SCL | | TIM3_CH1 | | | | | |
| P2.14 | SWCLK | | | | SPI_DI | SCL | | | | | | | |
| P2.15 | SWDIO | | | UART0_RXD | SPI_CS | SDA | | TIM2_CH1 | | | | CLUOUT1 | |

Table 3-11 LKS32MC07X Pin Function Selection (continued)

| Port | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P3.0 | | | | | | | | | | | | | OPA1_IP |
| P3.1 | | | | | | | | | | | | | OPA1_IN |
| P3.2 | | | MCPWM_CH3P | | | | | | | | | CLUOUT2 | |
| P3.3 | | | | | | | | | | | | | |
| P3.4 | | | MCPWM_CH3N | | | | | | | | | | |
| P3.5 | | | | | | | | | | | | | OPA0_IP |
| P3.6 | | | | | | | | | | | | | |
| P3.7 | | | | | | | | | | | | | OPA0_IN |
| P3.8 | | | | | | | | | | | | | |
| P3.9 | | | | UART1_TXD | | | | TIM3_CH1 | | | | | OSC_OUT |
| P3.10 | | | MCPWM_CH4P | | | | | | | | | | OPA2_IP |
| P3.11 | | | MCPWM_CH4N | | | | | | | | | | OPA2_IN |
| P3.12 | | | | | | | | | | | | | |
| P3.13 | | | | | | | | | | | | | |
| P3.14 | | | | | | | | | | | | | OPA3_IN |
| P3.15 | | | | | | | | | | | | | OPA3_IP |

# 4 Package size

## 4.1 LKS32MC070RBT8

LQFP64 Profile Quad Flat Package:

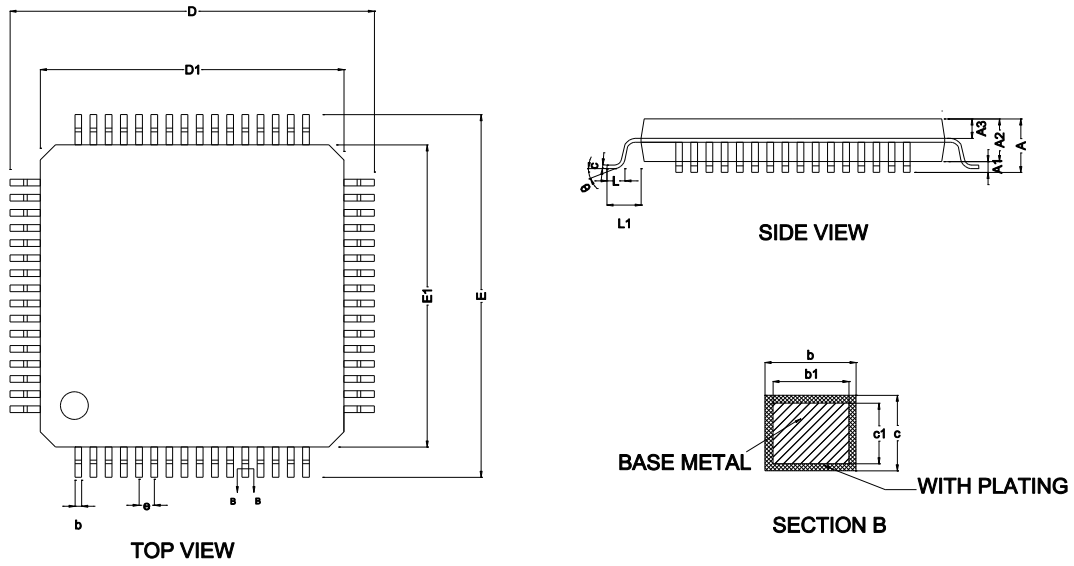



Fig.4-1 LKS32MC070RBT8 Package Diagram

Table 4-1 LKS32MC070RBT8 Package Size

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | - | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | - | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 11.80 | 12.00 | 12.20 |
| D1 | 9.90 | 10.00 | 10.10 |
| E | 11.80 | 12.00 | 12.20 |
| E1 | 9.90 | 10.00 | 10.10 |
| e | 0.50BSC | | |
| L | 0.45 | - | 0.75 |
| L1 | 1.00REF | | |
| θ | 0 | - | 7° |

## 4.2 LKS32MC071CBT8/LKS32MC071C8T8

TQFP48 Profile Quad Flat Package:

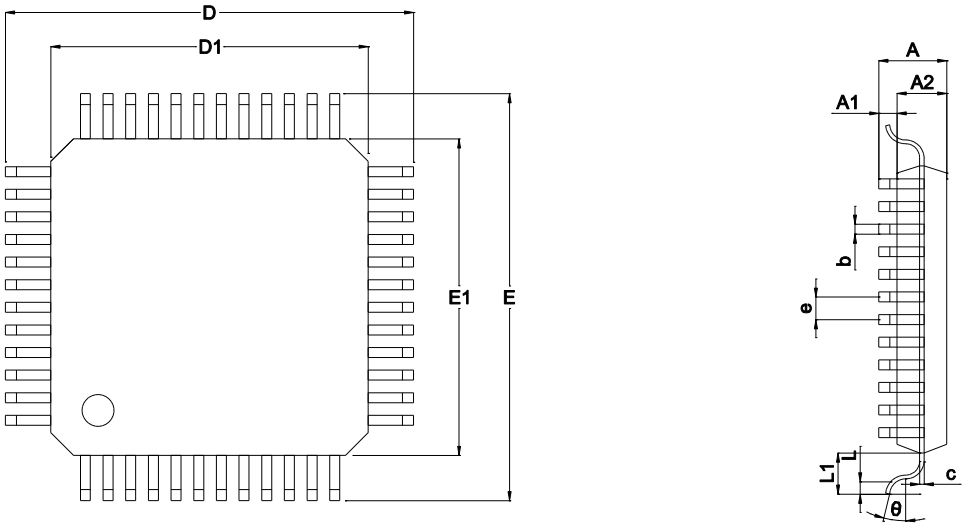
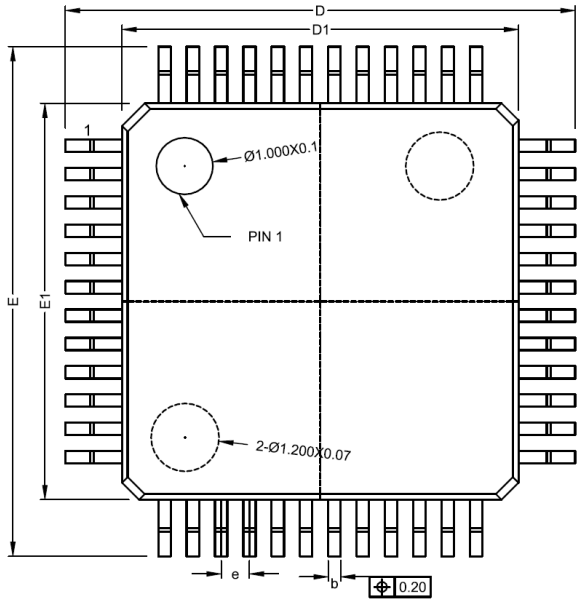


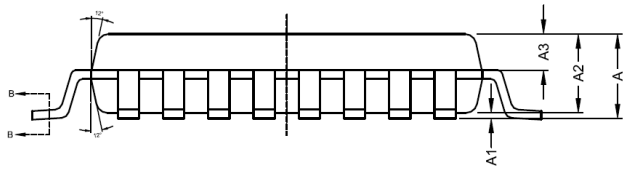

Fig.4-2 LKS32MC071CBT8/LKS32MC071C8T8 Package Diagram(TQFP48)

Table 4-2 LKS32MC071CBT8/LKS32MC071C8T8 Package Size(TQFP48)

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 1.20 |
| A1 | 0.05 | - | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.18 | 0.22 | 0.26 |
| c | 0.13 | - | 0.17 |
| D | 8.80 | 9.00 | 9.20 |
| D1 | 6.90 | 7.00 | 7.10 |
| E | 8.80 | 9.00 | 9.20 |
| E1 | 6.90 | 7.00 | 7.10 |
| e | - | 0.50 | - |
| θ | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 |
| L1 | - | 1.00 | - |




**TOP VIEW**




**SIDE VIEW**

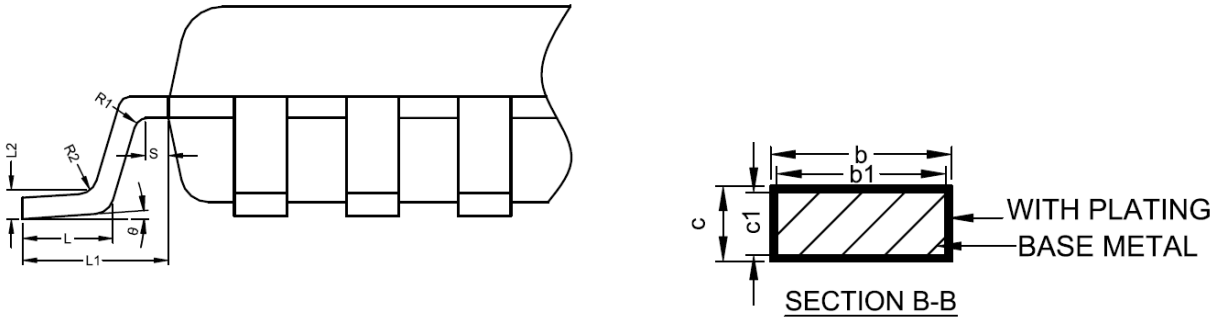



图 4-3 LKS32MC071CBT8/LKS32MC071C8T8 Package Diagram(LQFP48)

表 4-3 LKS32MC071CBT8/LKS32MC071C8T8 Package Size(LQFP48)

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 1.60 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |

| | | | |
|---|---|---|---|
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | - | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | - | 0.18 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 8.80 | 9.00 | 9.20 |
| D1 | 6.90 | 7.00 | 7.10 |
| E | 8.80 | 9.00 | 9.20 |
| E1 | 6.90 | 7.00 | 7.10 |
| e | 0.50BSC | | |
| L | 0.45 | - | 0.75 |
| L1 | 1.00REF | | |
| L2 | 0.25BSC | | |
| R1 | 0.08 | - | - |
| R2 | 0.08 | - | 0.20 |
| S | 0.20 | - | - |
| θ | 0° | 3.5° | 7° |

## 4.3 LKS32MC072KBQ8

QFN5*5 32L-0.75 Profile Quad Flat Package:

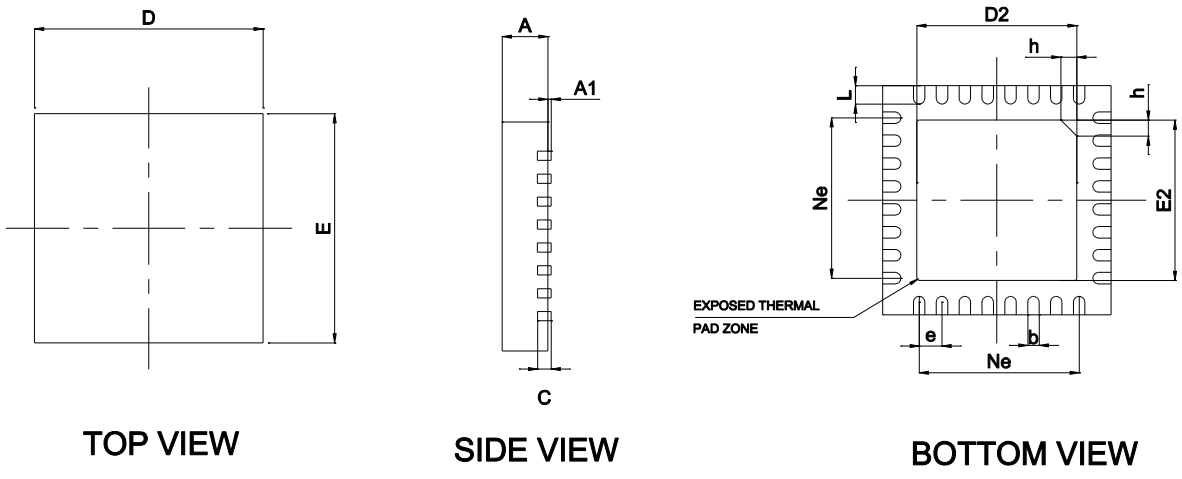



Fig.4-3 LKS32MC072KBQ8 Package Diagram

Table 4-3 LKS32MC072KBQ8 Package Size

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | - | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| c | 0.18 | 0.20 | 0.24 |
| D | 4.90 | 5.00 | 5.10 |
| D2 | 3.40 | 3.50 | 3.60 |
| e | 0.50BSC | | |
| Ne | 3.50BSC | | |
| E | 4.90 | 5.00 | 5.10 |
| E2 | 3.40 | 3.50 | 3.60 |
| L | 0.35 | 0.40 | 0.45 |
| h | 0.30 | 0.35 | 0.40 |

## 4.4 LKS32MC072KBT8

LQFP32 Profile Quad Flat Package:

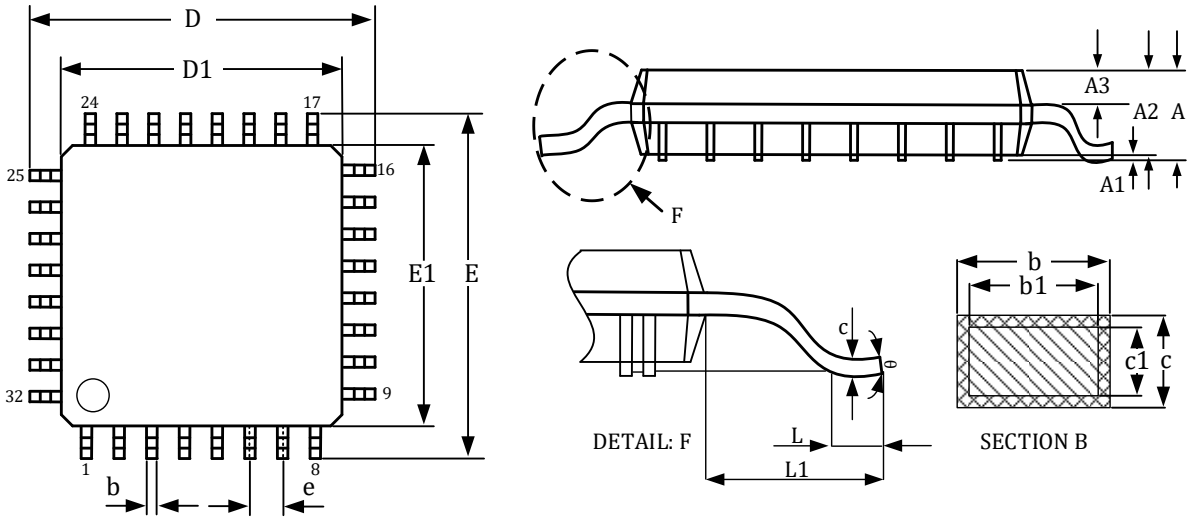



Fig.4-4 LKS32MC072KBT8 Package Diagram

Table 4-4 LKS32MC072KBT Package Size

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 1.70 |
| A1 | 0.05 | 0.1 | 0.2 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.32 | 0.37 | 0.42 |
| b1 | - | 0.35 | - |
| c | 0.09 | 0.145 | 0.20 |
| c1 | - | 0.125 | - |
| D | 8.80 | 9.00 | 9.20 |
| D1 | 6.90 | 7.00 | 7.10 |
| E | 8.80 | 9.00 | 9.20 |
| E1 | 6.90 | 7.00 | 7.10 |
| e | 0.80BSC | | |
| L | 0.30 | 0.50 | 0.70 |
| L1 | 1.00REF | | |
| θ | 0 | - | 8° |

## 4.5 LKS32MC073HBQ8

QFN3*3 20L-0.75 Profile Quad Flat Package:

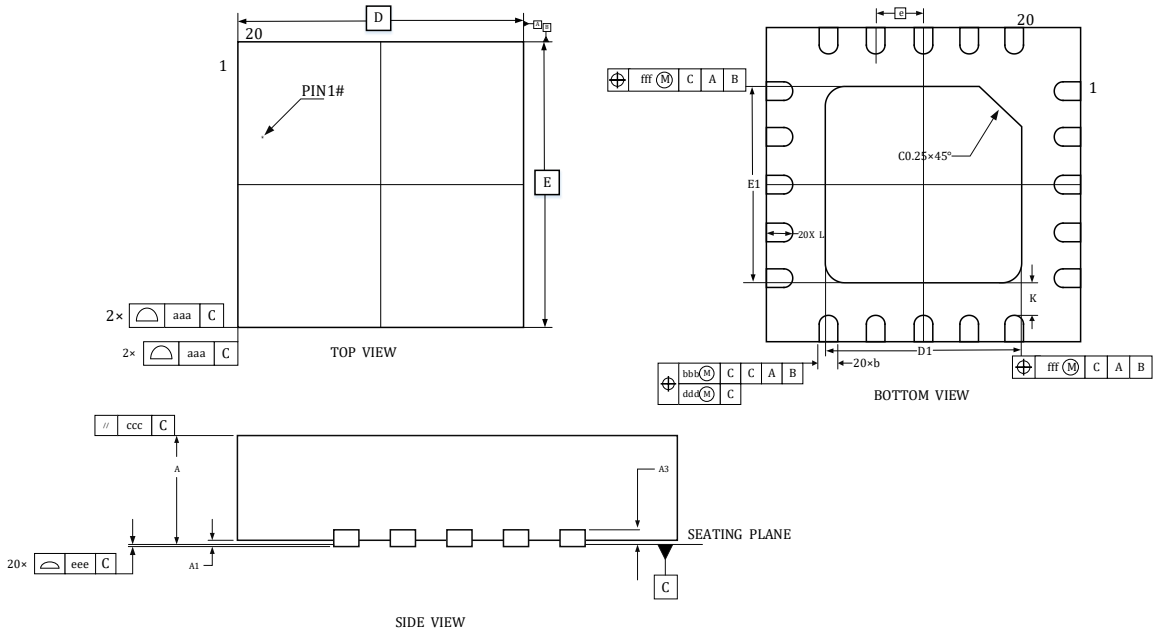



Fig.4-5 LKS32MC073HBQ8 Package Diagram

Table 4-5 LKS32MC073HBQ8 Package Size

| SYMBOL | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | 0.50 | 0.55 | 0.60 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | - | 0.152 REF | - |
| b | 0.15 | 0.20 | 0.25 |
| D | 3.00BSC | | |
| E | 3.00BSC | | |
| D1 | 1.60 | 1.70 | 1.80 |
| E1 | 1.60 | 1.70 | 1.80 |
| e | 0.40BSC | | |
| L | 0.25 | 0.30 | 0.35 |
| K | 0.20 | - | - |
| aaa | 0.10 | | |
| bbb | 0.07 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

## 4.6 LKS32MC077MBS8

SSOP24L Profile Quad Flat Package:

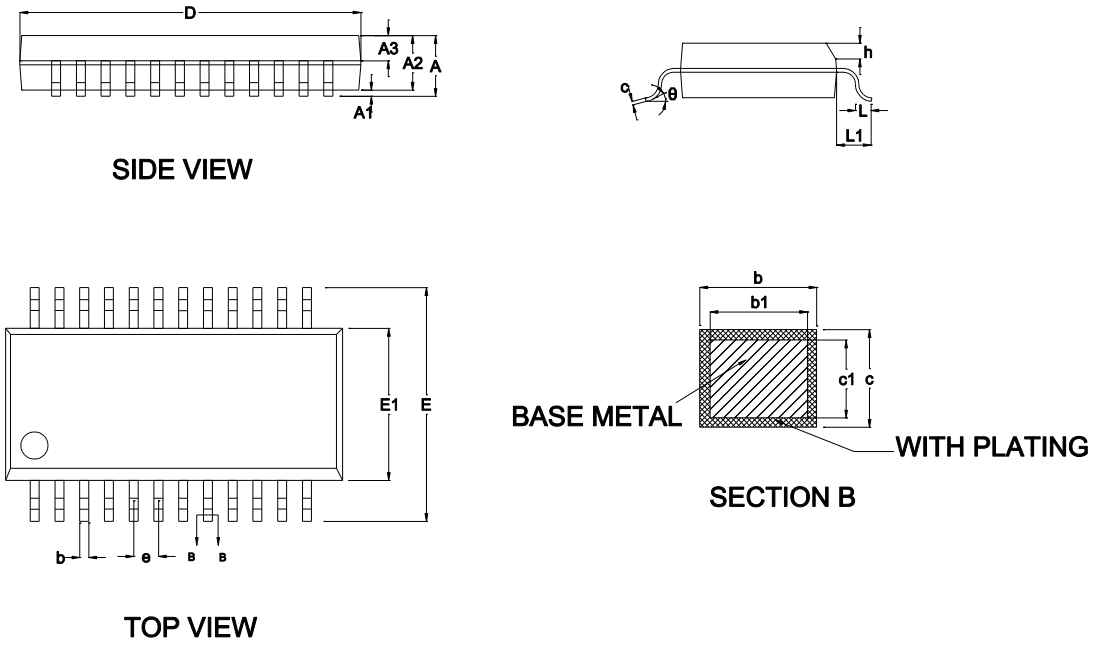



Fig.4-6 LKS32MC077MBS8 Package Diagram

Table 4-6 LKS32MC077MBS8 Package Size

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 1.75 |
| A1 | 0.10 | 0.15 | 0.25 |
| A2 | 1.30 | 1.40 | 1.50 |
| A3 | 0.60 | 0.65 | 0.70 |
| b | 0.23 | - | 0.31 |
| b1 | 0.22 | 0.25 | 0.28 |
| c | 0.20 | - | 0.24 |
| c1 | 0.19 | 0.20 | 0.21 |
| D | 8.55 | 8.65 | 8.75 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 0.635BSC | | |
| h | 0.30 | - | 0.50 |
| L | 0.50 | - | 0.80 |
| L1 | 1.05REF | | |
| θ | 0 | - | 8° |

*Support IEC/UL60730 functional security certification

# 5 Electrical performance parameters

Table 5-1 LKS32MC07x electrical absolute characteristics

| Parameter | Min. | Max. | Unit | Explain |
|---|---|---|---|---|
| MCU Power Supply Voltage (AVDD) | -0.3 | +6.0 | V | |
| Gate Driver Power Supply Voltage (VCC) | -0.3 | +25.0 | V | LKS07x with 6N driver |
| | -0.3 | +40.0 | V | LKS07x with 3P3N driver |
| Supply Voltage (VCCLDO) | -0.3 | +25.0 | V | Pin for LDO supply in 074do |
| Operating temperature | -40 | +105 | ˚C | |
| Storage temperature | -40 | +150 | ˚C | |
| Junction temperature | - | 125 | ℃ | |
| Pin temperature (soldering for 10 seconds) | - | 260 | ℃ | |

Table 5-2 LKS32MC07x Recommended working condition parameters

| Parameter | Mini. | Typ. | Max. | Unit | Explain |
|---|---|---|---|---|---|
| MCU Power Supply Voltage (AVDD) | 2.5 | 5 | 5.5 | V | |
| Analog Power Supply Voltage ($AVDD_A$) | 2.8 | 5 | 5.5 | V | REF2VDD = 0, ADC selects 2.4 V internal reference |
| | 2.4 | 5 | 5.5 | V | REF2VDD = 1, ADC selects AVDD as reference |

Table 5-3 LKS32MC07x ESD Parameters

| Item | Minimal | Max | Unit |
|---|---|---|---|
| ESD Test (HBM) | -6000 | 6000 | V |

According to "MIL-STD-883J Method 3015.9", under the environment of 25℃ and 55% relative humidity, electrostatic discharge is applied to all IO pins of the tested chip for 3 times, with an interval of 1s each time. The test results show that the anti-static discharge level of the chip reaches Class 3A ≧4000V, <8000V.

Table 5-4 LKS32MC07x Latch-up parameters

| Item | Minimal | Max | Unit |
|---|---|---|---|
| Latch-up current (85 ℃) | -200 | 200 | mA |

According to "JEDEC STANDARD NO.78E NOVEMBER 2016", an overvoltage of 8 V is applied to all power supply IOs, and a current of 200 ma is injected on each signal IO. The test results show that the anti-latch-up level of the chip is 200 mA.

Table 5-5 LKS32MC07x IO absolute characteristics

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{IN}$ | GPIO Signal Input Voltage Range | -0.3 | 6.0 | V |
| $I_{INJ\_PAD}$ | Maximum Injection Current of A Single GPIO | -11.2 | 11.2 | mA |
| $I_{INJ\_SUM}$ | Maximum Injection Current of All GPIOs | -50 | 50 | mA |

Table 5-6 LKS32MC07x IO DC Parameters

| Parameter | Description | AVDD | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High input level of digital IO | 5V | - | 3.06 | | V |
| | | 3.3V | | 2.07 | | |
| $V_{IL}$ | Low input level of digital IO | 5V | - | | 0.3*AVDD | V |
| | | 3.3V | | | 0.8 | |
| $V_{HYS}$ | Schmidt hysteresis range | 5V | - | 0.1*AVDD | | V |
| | | 3.3V | | | | |
| $I_{IH}$ | Digital IO current consumption when input is high | 5V | - | | 1 | uA |
| | | 3.3V | | | | |
| $I_{IL}$ | Digital IO current consumption when input is low | 5V | - | -1 | | uA |
| | | 3.3V | | | | |
| $V_{OH}$ | High output level of digital IO | | Current = 11.2mA | AVDD-0.8 | | V |
| $V_{OL}$ | Low output level of digital IO | | Current = 11.2mA | | 0.5 | V |
| $R_{pup}$ | Pull-up resistor* | | | 11 | 13 | kΩ |
| $R_{io\text{-}ana}$ | Connection resistance between IO and internal analog circuit | | | 100 | 200 | Ω |
| $C_{IN}$ | Digital IO Input-capacitance | 5V | - | | 10 | pF |
| | | 3.3V | | | | |

Table 5-7 LKS32MC07x Module Current/IDD

| 模块 | Min | Typ | Max | 单位 |
|---|---|---|---|---|
| Comparator x1 | | 0.005 | | mA |
| OPA x1 | | 0.450 | | mA |
| ADC | | 3.710 | | mA |
| DAC | | 0.710 | | mA |
| Temp Sensor | | 0.150 | | mA |
| Band-Gap | | 0.154 | | mA |
| 4MHz RC Clock | | 0.105 | | mA |
| PLL | | 0.080 | | mA |
| CPU+flash+SRAM (96MHz) | | 8.667 | | mA |
| CPU+flash+SRAM (12MHz) | | 1.600 | | mA |
| CRC | | 0.070 | | mA |
| DSP | | 3.421 | | mA |
| UART | | 0.107 | | mA |
| DMA | | 1.340 | | mA |
| MCPWM | | 0.053 | | mA |

| | | | | |
|---|---|---|---|---|
| TIMER | | 0.269 | | mA |
| SPI | | 0.500 | | mA |
| IIC | | 0.500 | | mA |
| CAN | | 2.200 | | mA |
| Sleep Mode | 9 | 12 | 20 | uA |

Unless otherwise noted, the above tests are conducted under the condition of 25 ° 5V power supply at room temperature and 96MHz clock. Due to the device model deviation in the manufacturing process, the current consumption of different chips will be different.

# 6 Analog Characteristics

Table 6-1 LKS32MC07x analog characteristics

| Parameter | Min. | Typ. | Max. | Unit | Explain |
|---|---|---|---|---|---|
| **MCU** | | | | | |
| Power Supply Voltage | 2.5 | 5 | 5.5 | V | |
| **Analog-to-digital converter (ADC)** | | | | | |
| Power Supply | 3.3 | 5 | 5.5 | V | ADC use 2.4V internal reference |
| | 2.8 | 5 | 5.5 | V | ADC use 1.2V internal reference |
| Sampling rate | | 3 | | MHz | fadc/16 |
| Differential Input Signal Range | -5.0<br>+0.144 | | +5.0<br>-0.144 | V | When ADCx_GAIN = 1; REF=2.4V |
| | -3.6<br>+0.072 | | +3.6<br>-0.072 | V | When ADCx_GAIN = 0; REF=2.4V |
| Single-ended Input Signal Range | -0.3 | | AVDD<br>+0.3 | V | Limited by the input voltage of the IO port |
| The differential signal is usually the signal output from the OPA inside the chip to the ADC; Sin-gle-ended signals are typically sampled externally via an I0 input: The ADC should measure the signal amplitude no more than ±98% of the full scale, regardless of the internal/external reference used. In particular, when using an external reference, it is recommended that the sampling con-ductor not exceed 90% of the scale. | | | | | |
| DC offset | | 5 | 10 | mV | Correctable |
| Effective number of bits (ENOB) | 10.5 | 11 | | bit | |
| INL | | 2 | 3 | LSB | |
| DNL | | 1 | 2 | LSB | |
| SNR | 63 | 66 | | dB | |
| Input Re-sistance | 500k | | | Ohm | |
| Input Capaci-tance | | 10 | | pF | |
| **Reference Voltage (REF)** | | | | | |
| Power Supply | 2.2 | 5 | 5.5 | V | |
| Output Devia-tion | -9 | | 9 | mV | |
| Rejection Ratio of Power Sup- | | 70 | | dB | |

| Parameter | Min. | | Typ. | Max. | Unit | Explain |
|---|---|---|---|---|---|---|
| **MCU** | | | | | | |
| Power Supply Voltage | 2.5 | | 5 | 5.5 | V | |
| ply | | | | | | |
| Temperature Coefficient | | | 20 | | ppm/°C | |
| Output Voltage | | | 1.2 | | V | |
| **Digital-to-Analog Converter (DAC)** | | | | | | |
| Power Supply | 2.2 | | 5 | 5.5 | V | |
| Load Resistance | 5k | | | | Ohm | Output BUFFER is on |
| Load capacitance | | | | 50p | F | |
| Output voltage range | 0.05 | | | AVDD-0.1 | V | |
| Conversion speed | | | | 1M | Hz | |
| DNL | | | 1 | 2 | LSB | |
| INL | | | 2 | 4 | LSB | |
| OFFSET | | | 5 | 10 | mV | |
| SNR | 57 | | 60 | 66 | dB | |
| **Operational Amplifier (OPA)** | | | | | | |
| Power Supply | 2.8 | | 5 | 5.5 | V | |
| Bandwidth | | | 10 | 20 | MHz | |
| Load Resistance | 20k | | | | Ohm | |
| Load Capacitance | | | | 5p | F | |
| Input Common Mode Voltage Range (VICM) | 0 | | | AVDD | V | |
| Output Signal Range | 0 | | | 2Vcm | V | Under minimum load resistance |
| Common Mode Voltage (Vcm) | 1.45 | 1.8 | 2.2 | V | 32 times | Measurement condition: normal temperature. Operational amplifier swing=2 × min(AVDD-Vcm, Vcm). It is recommended that the application using OPA single output should be powered on to measure Vcm and make software subtraction correction. |
| | 1.5 | 1.8 | 2.2 | V | 16 times | |
| | 1.55 | 1.8 | 2.2 | V | 8 times | |
| | 1.6 | 1.8 | 2.2 | V | 4 times | |

| Parameter | Min. | Typ. | Max. | Unit | Explain |
|---|---|---|---|---|---|
| **MCU** | | | | | |
| Power Supply Voltage | 2.5 | 5 | 5.5 | V | |
| | | | | | For more analysis, please refer to the official website application note "ANN009 - Differences between Operational Amplifier Differential and Single Operating Mode". |
| OFFSET | | 10 | 15.0 | mV | 32 times |
| | | 10 | 16.5 | mV | 16 times |
| | | 10 | 18.5 | mV | 8 times |
| | | 10 | 20.5 | mV | 4 times |
| This OFFSET is the equivalent differential input deviation obtained when the OPA differential input is short-circuited and OPA OUT is measured from 0 level. The output deviation of OPA is OPA magnification x OFFSET. The Flash NVR area records the OPA offset for factory tests. | | | | | |
| Common Mode Rejection Ratio (CMRR) | | 80 | | dB | |
| Power Supply Rejection Ratio (PSRR) | | 80 | | dB | |
| Load Current | | | 500 | uA | |
| Slew Rate | | 5 | | V/us | |
| Phase Margin (PM) | | 60 | | Degree | |
| **Comparator (CMP)** | | | | | |
| Power Supply | 2.2 | 5 | 5.5 | V | |
| Input Signal Range | 0 | | AVDD | V | |
| OFFSET | -36 | -10 | 12 | mV | 0 mV hysteresis, CMP output transitions from low to high |
| | -36 | -10 | 12 | mV | 0 mV hysteresis, CMP output transitions from high to low |
| | -14.5 | -10 | 33.5 | mV | 20 mV hysteresis, CMP output transitions from low to high |
| | -14.5 | 11.5 | 33.5 | mV | 20 mV hysteresis, CMP output transitions from high to low |
| Delay | | 50 | | nS | Default power consumption |
| | | 200 | | nS | Low power consumption |
| Hysteresis | | 20 | | mV | HYS='0' |
| | | 0 | | mV | HYS='1' |

Analog register table description:

The names of the analog registers are SYS_AFE_REG0 to SYS_AFE_REG6, corresponding to addresses 0x4000 0010 to 0x4000_0028. Address 0x4000_001C to 0x4000_0028 are the calibration registers of each analog module. These registers will fill their respective calibration values into the Flash info area before leaving the factory, and will be automatically loaded to the SYS _ AFE _ REG3 to SYS _ AFE _ REG6 after power-on. In general, the user should not configure or change these values. If fine-tuning is required, please read the original settings first, and then adjust based on those values.

Addresses space of 0x4000_0000 to 0x4000_0018 are registers open to users. The blank registers must be configured to 0 (these registers will be reset to 0 after power on). Other registers could be configured in situations.

# 7 Power management system

The power management system is composed of LDO15 module, power detection module (PVD), power-on/power-off reset module (POR).

AVDD is powered by a 2.5V ~ 5.5V supply, and all internal digital circuits and PLL modules are powered by an internal LDO15.

The LDO15 is automatically turned on after power-on. No software configuration is necessary. And the LDO15 output voltage can be adjusted by software.

The output voltage of LDO15 can be adjusted by setting register LDO15TRIM<2:0>. The corresponding value of the register can be seen in the analog register table. LDO15 has been calibrated before it leaves the factory. Generally, users do not need to configure these registers again. If fine-tuning of the LDO output voltage is required, please read the original configuration value first, and then calculate the new settings accordingly.

The POR module monitors the voltage of the LDO15. When the voltage of the LDO15 is lower than 1.26V, for example, at the beginning of power-on or at the time of power-off, it will provide a reset signal for the digital circuit to avoid any abnormal operation.

The PVD module monitors the 5V input power. If it is below a certain threshold, it will remind the MCU by sending an alarm (interrupt) signal. The interrupt reminder threshold can be set to different voltages through the PVDSEL<1:0> registers. The PVD module can be turned off by setting PD_PDT = '1'. For the corresponding value of specific register, please refer to the analog register table.

# 8 Clock system

The clock system consists of a 32KHz RC oscillator, a 8MHz RC oscillator, an external 8MHz crystal oscillator, and a PLL.

The 32K RC clock is used in the MCU system as a slow clock for modules such as reset/wakeup source filters or used in the low power mode; The 8MHz RC clock can be used as the main clock of the MCU, and can provide a reference clock to PLL. PLL clock is up to 96MHz; The external 8MHz crystal oscillator is used as a backup clock.

Both 32k and 8M RC clocks will been through factory calibration. In the range of -40 ~ 105 ℃, the accuracy of the 32K RC clock is ±50%, and the accuracy of the 8M RC clock is ± 1%.

The frequency of the 32K RC clock can be set by the register RCLTRIM<3:0>, and the frequency of the 8M RC clock can be set by the register RCHTRIM <5:0>. For the corresponding value of specific register, please refer to the analog register table.

The chip has been calibrated before it leaves the factory. Generally, users do not need to configure these registers again. If fine-tuning of the frequency is required, please read the original configuration value first, and then calculate the new settings accordingly.

The 8M RC clock is turned on by setting RCHPD = ’0’ (ON by default, turn off when set to “1’). The RC clock needs a reference voltage and current provided by the Bandgap voltage reference module; thus, do remember to turn on the BGP module before turning on the RC clock. When the chip is powered on, the 8M RC clock and BGP module are both turned on automatically. The 32K RC clock is always on and cannot be turned off.

The PLL multiplies the 8M RC clock to provide a higher frequency clock for modules like MCU and ADC. The highest frequency of MCU and PWM module is 96MHz, and the typical working frequency of ADC module is 48MHz. It can be set to different frequency by the register ADCLKSEL <1:0>.

PLL is turned on by setting PLLPDN = ’1’ (OFF by default, turn on when set to '1'). Before turning on the PLL module, the BGP (Bandgap) module should be turned on first. After the PLL is turned on, it needs a settling time of 6us to achieve a stable frequency output. When the chip is powered on, the RCH clock and BGP module are both turned on. PLL is OFF by default and could be enabled by software.

The crystal oscillator circuit has a built-in amplifier and an oscillator capacitor. Connect a crystal between IO OSC_IN/OSC_OUT and set XTALPDN = ’1’ to start the oscillation.

# 9 Voltage Reference

Reference voltage and current are provided for ADC, DAC, RC clock, PLL, temperature sensor, operational amplifier, comparator and FLASH. Before using any of the above modules, the BGP voltage reference should be turned on first.

When the chip is powered on, the BGP module is turned on automatically. The voltage reference is turned on by setting BGPPD = '0'. From OFF to ON, BGP needs about 6us to stabilize. BGP output voltage is about 1.2V, and accuracy is ± 0.8%.

# 10 ADC module

The chip integrated a synchronous double-sampling SAR ADC which is shut down by default when the chip is powered up. Before turning on ADC, the BGP module, 8M RC clock and PLL should be turned on first. In the default configuration, ADC clock is 48MHz, which corresponds to a conversion rate of 3Msps.

The synchronous double sampling circuit can sample the two input analog signals at the same time. After the sampling is completed, the ADC converts the two signals one by one and writes them into the corresponding data registers.

ADC takes 16 ADC clock cycles to complete one conversion, of which 13 are conversion cycles and 3 are sampling cycles. I.E. $f_{conv}=f_{adc}/16$. When the ADC clock is set to 48MHz, the conversion rate is 3Msps.

When the ADC is working at a lower frequency, the power consumption can be reduced by setting register CURRIT<1:0>.

ADC could work in different modes: One-time single channel trigger mode, continuous single channel sampling mode, One-time 1 to 20 channels scanning mode, continuous 1 to 20 channels scanning mode. It has a set of 20 independent registers for each analog channel.

The ADC trigger can be MCPWM/Timer trigger signals T0, T1, T2 and T3 happened for the preset number of times, or software trigger event.

ADC _ DC stores the DC offset of ADC. Usually, in the calibration phase, the ADC DC offset value is obtained by measuring the AVSS (internal ground) of Channel 15 (counting from 0) and stored in flash. In the system loading phase, the DC offset is written into the ADC _ DC register by software.

The ADC has two ranges set by the ADC X _ GAIN (X = 0, 1): 3.6 V and 7.2 V. At the 7.2 V range, this corresponds to a maximum input signal amplitude of ± 5 V because the chip is powered at 5 V. At the 3.6 V range, this corresponds to a maximum input signal amplitude of ± 3.6 V. When measuring the output signal of an op amp, select the specific ADC gain based on the maximum signal that the op amp can output.

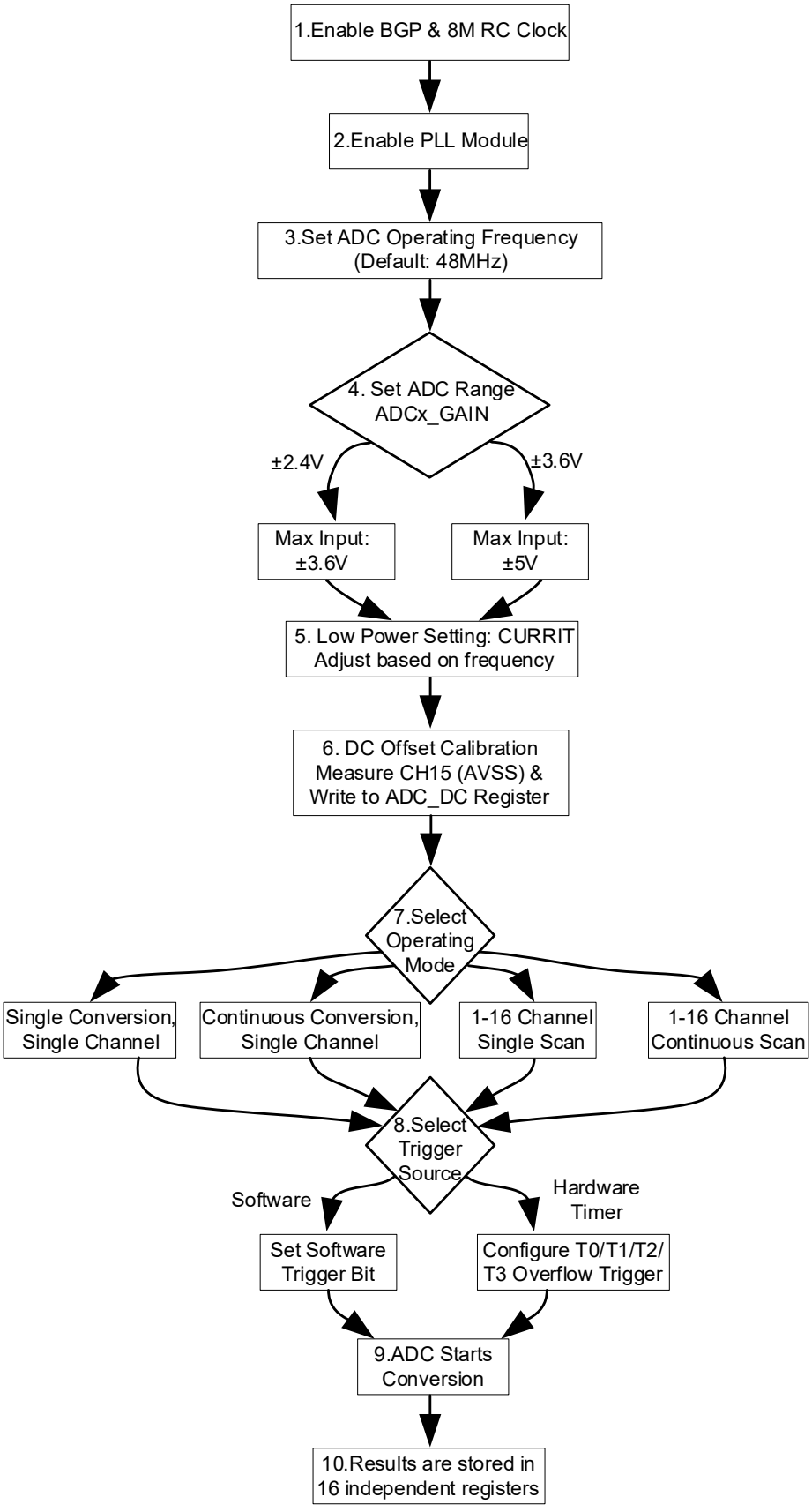



Figure 10-1ADC Configuration Flowchart

# 11 SPI module

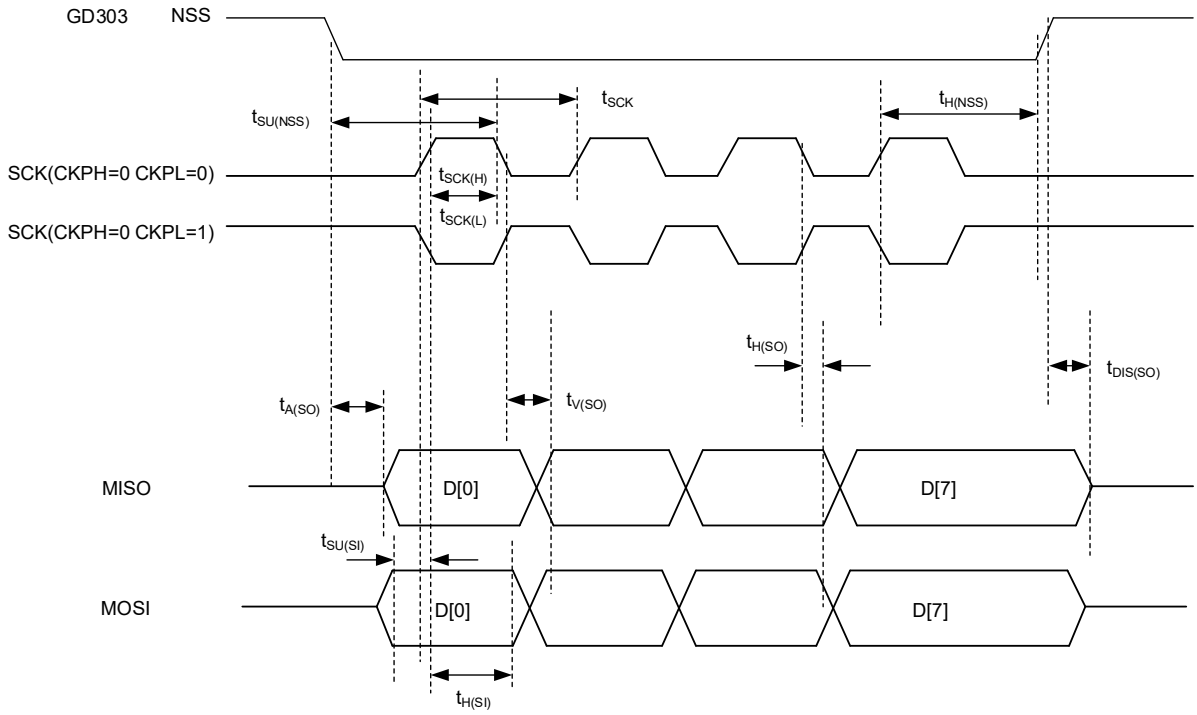



图 11-1 SPI Slave Mode Timing Diagram

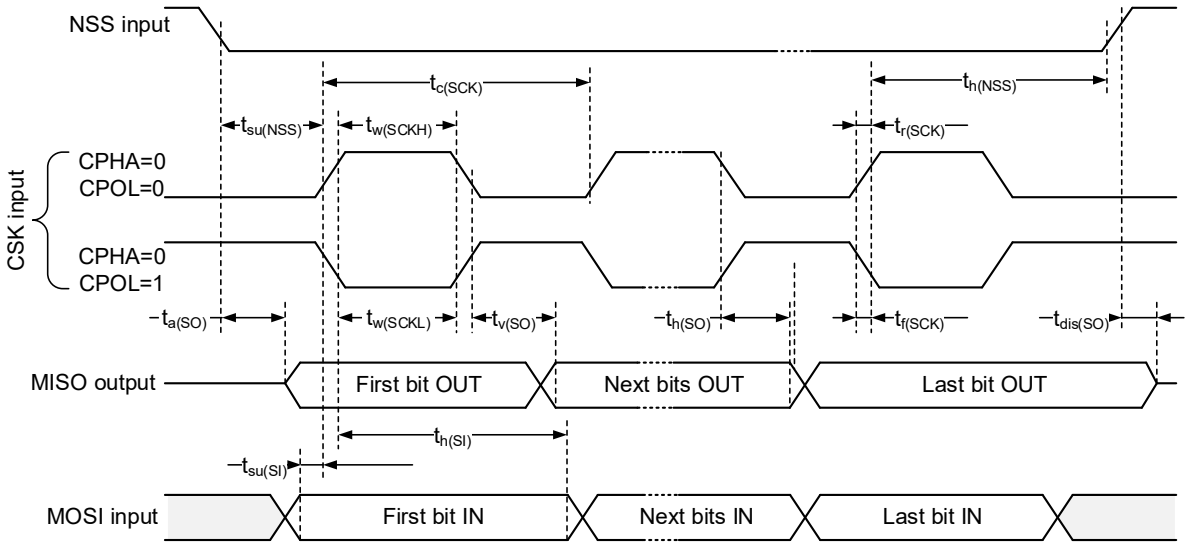



图 11-2 SPI Slave Mode Timing Diagram with CHPA=0

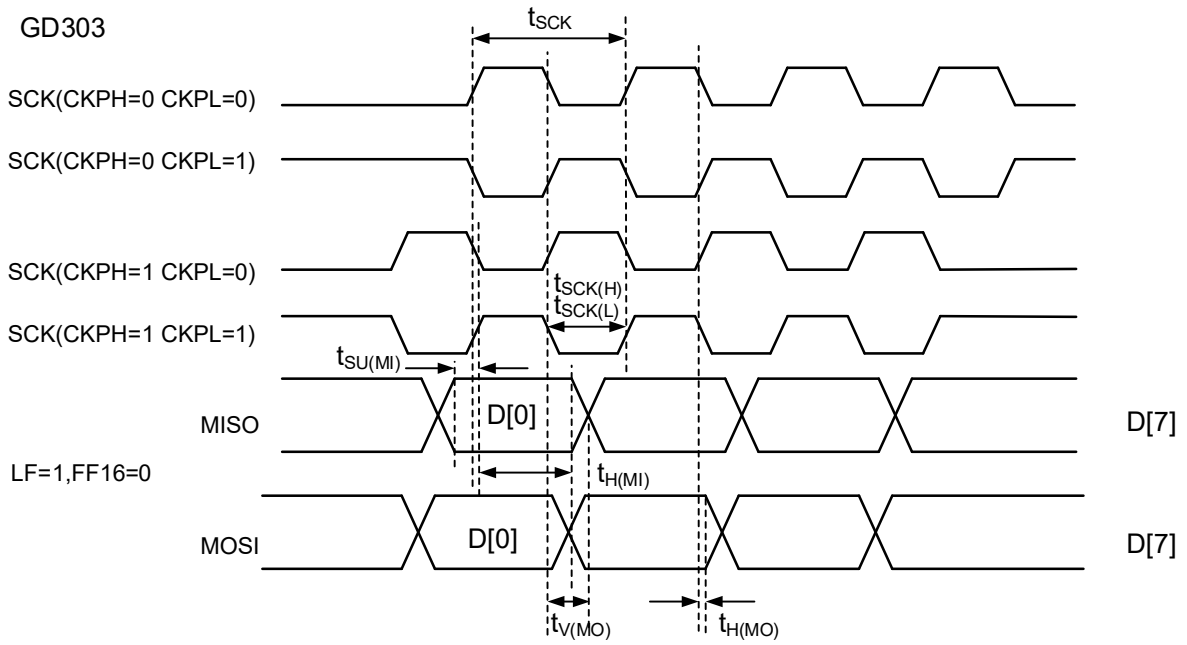



图 11-3 SPI Master Mode Timing Diagram

Table 11-1 SPI Timing Parameters Table

SPI mode, polarity 0, phase 0, rising edge sampling, falling edge output

| Parameter | Min. | Typical | Max. | Unit | Description |
|---|---|---|---|---|---|
| $f_{SCK}$ | — | — | 12 | MHz | Theoretical value, with a 1% margin of error in actual measurements. The maximum allowable baud rate is 12 MHz. |
| $t_{SCK(H)}$ | 41.25 | 41.67 | 42.09 | nS | Half SCK cycle |
| $t_{SCK(L)}$ | 41.25 | 41.67 | 42.09 | nS | Half SCK cycle |
| **SPI master mode** | | | | | |
| $t_{V(MO)}$ | — | 9.9 | 10 | nS | CLK falling edge to MOSI new data start validity |
| $t_{H(MO)}$ | 2 | — | — | nS | CLK falling edge to MOSI old data start transition |
| $t_{SU(MI)}$ | -25 | — | — | nS | MISO to CLK rising edge setup time requirement |
| $t_{H(MI)}$ | 40 | — | — | nS | MISO to CLK rising edge hold time requirement |
| **SPI slave mode** | | | | | |
| $t_{SU(NSS)}$ | 20 | — | — | nS | The chip select signal is pulled low at the first rising edge of CLK. |
| $t_{H(NSS)}$ | -40 | — | — | nS | The rising edge of the last CLK signal pulls the chip select high. |
| $t_{A(SO)}$ | 51.5 | — | 52.5 | nS | Lower the frame selection to MISO to begin sending data. |
| $t_{DIS(SO)}$ | 47.5 | — | 48.5 | nS | Raise the selection to MISO 0 |
| $t_{V(SO)}$ | — | 38 | 38.4 | nS | From the falling edge of CLK to the completion of new data transmission |
| $t_{H(SO)}$ | 29.2 | — | — | nS | From the falling edge of CLK to the start of old data change |

| | | | | | |
|---|---|---|---|---|---|
| $t_{SU(S)}$ | -20 | — | — | nS | From MOSI signal stabilization to the rising edge of CLK |
| The chip operates at 3.3V and was tested at a clock frequency of 96MHz (when powered at 5V, significant ringing appears on the oscilloscope probe; probe cable length is 1m). | | | | | |

# 12 Operational Amplifier

4-channel of rail-to-rail OPAs are integrated, with a built-in feedback resistor R2/R1. A resistor R0 is required to be connected in series to the external pin. The resistance of feedback resistors R2:R1 can be adjusted by register RES_OPA0<1:0> to achieve different gain. For the corresponding value of specific register, please refer to the analog register table.

The close-loop gain of OPA is R2/(R1+R0), where R0 is the resistance of the external resistor.

For the application of MOS resistance direct sampling, it is recommended to connect an external resistance of >20kΩ to reduce the current flowing into the chip pin when the MOS is turned off;

For the application of small resistance sampling, it is recommended to connect an external resistor of 100Ω.

The OPA can select one of the output signals of the 4-channels amplifiers by setting OPAOUT_EN <2:0>, and send it to the P2.7 IO port through a buffer for measurement (see the corresponding relationship in the datasheet 'Pin Function Description" ). Because of this buffer, the OPA is able to be output to an IO while operating normally.

When the chip is powered on, the OPA module is OFF by default. It can be turned on by setting OPAxPDN = ’1’, and turn on the BGP module before turning on the amplifier.

For built-in clamp diodes are integrated between the positive and negative OPA inputs, the motor phase line could be directly connected to the OPA input through a matching resistor, thereby simplifying the external circuit for MOSFET current sampling.

# 13 Comparator

Built-in 3-channel rail-to-rail comparators with programmable comparator speed, hysteresis voltage, and signal source.

The comparison delay of the comparator can be set to < 30nS/200 nS through Register CMP _ FT. The hysteresis voltage is set to 20 mV/0 mV by the CMP _ HYS.

The comparator positive input signal source can be set by register CMPx _ SELP [2:0]; the comparator negative input signal source can be set by register CMPx _ SELN [1:0] (X = 0/1/2 for comparators CMP0/CMP1/CMP2）。

When the chip is powered on, the comparator module is OFF by default. The comparator is turned on by setting CMPxPDN = ’1’, and turn on the BGP module before turning on the comparator.

# 14 Temperature sensor

The chip has a temperature sensor with an accuracy of ±2°C. The temperature sensor will be calibrated in factory, and the calibration value is saved in the flash info area.

When the chip is powered on, the temperature sensor module is OFF by default. Turn on the BGP module before turning on the temperature sensor.

The temperature sensor is turned on by setting TMPPDN = ’1’, and it takes about 2us to be stable after turning on. Thus, it should be turned on at least 2us ahead before the ADC measures the sensor output.

# 15 DAC module

The chip contains two 12-bit DACs, and the maximum range of the output signal can be set to 1.2 V/4.85 V using the DAC0 _ GAIN and DAC1 _ GAIN registers.

DAC0 can route the DAC0 output to the P0.0 pin through the configuration register DAC0OUT _ EN = 1, and DAC1 can route the DAC1 output to the P0.0 pin through the configuration register DAC1OUT _ EN = 1, which can drive a load resistor of > 5kΩ and a load capacitance of 50pF. Normally, DAC0 and DAC1 are not output at the same time to avoid signal contention.

The maximum output bit rate of DAC is 1MHz.

When the chip is powered on, the DAC module is OFF by default. DAC0 can be turned on by setting DAC0PDN = 1, and DAC1 can be turned on by setting DAC1PDN = 1. Before turning on the DAC module, you need to turn on the BGP module.

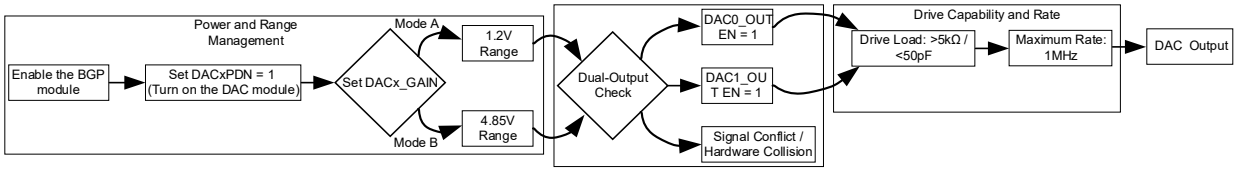



Figure 15-1DAC Configuration Flowchart

# 16 Processor core

- 32-bit Cortex-M0 + DSP dual-core processor
- Two-wire SWD debug pin
- System frequency is up to 96MHz

# 17 Storage resources

## 17.1 Flash

- built-in flash including 64kB/128kB main area and 1.5kB NVR
- Endurance: 100,000 Cycles(min)
- Data retention: more than 100 years
- Single byte program: 7.5us(max), Sector erase: 5ms(max)
- Sector size 512bytes, supporting Sector erase/program and in-application program
- Flash data anti-theft by programming the last word of flash to any words other than 0xFFFFFFFF

## 17.2 SRAM

- built-in 12kB SRAM

# 18 MCPWM for motor drive

- MCPWM operating frequency is up to 96MHz
- It can generate 6 pairs of non-overlapping PWM signals (complementary mode) or 12 independent non-overlapping PWM signals (edge-aligned mode). The module consists of two chopper modules, with each group sharing one dead-time configuration.
- Support edge-aligned PWM
- Support software control IO mode
- Support IO polarity control
- Internal short circuit protection to avoid short circuit due to configuration error
- External short circuit protection, enabling fast shutdown by monitoring the external signals
- Internal ADC sampling interrupt
- Preload MCPWM register configuration and update simutaneously
- Programmable load time and period

# 19 Timer

- 4-channel standard timer, 2-channel 16-bit timer, 2-channel 32-bit timer.
- Support capture mode for measuring external signal/pulse width
- Support comparison mode for timed interruption of edge-aligned PWM

In particular, LKS32MC070/ LKS32MC071/ LKS32MC072/ LKS32MC077 has 2 channels to support coded signal input and support pulse instruction counting.

# 20 Hall sensor interface

- Built-in 1024 cycles filtering
- 3-channel Hall signal input
- 24-bit counter, with overflow and capture interrupt

# 21 DMA

- One DMA engine
- Supporting up to 4 channels
- Supporting byte/halfword/word transfers of different sizes
- Supporting different address increment mode
- Supporting data transfer between flash/ram/peripherals
- Supporting cycle mode

# 22 DSP

- Customized DSP instruction set for motor control algorithm, , three-stage pipeline achitecture
- Operating frequency is up to 96MHz
- 32/16-bit divider, could finish one division calculation in 12 cycles（96MHz）
- 32-bit hardware SQRT, could finish one SQRT calculation in 8 cycles（96MHz）
- Q15 format Cordic trigonometric function module, could finish sin/cos/artanc calculation in 20 cycles（96MHz）
- DSP has independent program memory and data memory, DSP could execute its program independently, and can also be called by MCU to perform a certain calculation as a AHB slave like a coprocessor
- Support DSP IRQ and pause state for data exchange purpose with MCU

# 23 CRC

- Supporting polynomials of different bit widths such as 7/8/16/32
- Supporting polynomial coefficient configuration
- Supporting input and output data flipping

# 24 General Purpose Peripheral

- Two UART, full-duplex operation, support 8/9 data bit, 1/2 stop bit, odd/even/no parity mode, with 1 byte tx buffer, 1 byte rx buffer, support Multi-drop Slave/Master mode, support 300 to 115200 baud rate
- One SPI, support master-slave mode
- One IIC, support master-slave mode
- One CAN-bus
- Hardware watchdog, driven by 32kHz RC clock and which is independent of system high-speed clock, the minimum reset interval was 4096/32kHz≈128ms, and the maximum reset interval was 511×4096/32kHz≈64s.

Please refer to Section 2 Selection table for different types of peripherals.

# 25 Special IO multiplexing

Notes for Special IO Multiplexing of LKS07x

The SWD protocol includes two signals: SWCLK and SWDIO. SWCLK is a clock signal. To the chip, it is an input and will always be an input. SWDIO is a data signal. It switches between the input state and the output state during data transmission, and the default is the input state.

Some LKS07x SWD pins also have GPIO function. The IO multiplexed by SWCLK is P2.14 and the IO multiplexed by SWDIO is P2.15. The precautions are as follows:

- The default state of GPIO multiplexing is disabled, IO are used as SWD. After the hard reset of the chip, the initial state of IOs are SWD. Both IOs of SWD are fixed pull-up inside the chip (the internal pull-up resistor of the chip is about 12K). Please pay attention to the initial IO voltage level if application has specific requirements.
- When GPIO multiplexing is enabled, tools such as KEIL cannot directly access the chip, i.e., the Debug and erase download functions cannot access the chip since SWD are now general GPIO. If the program needs to be downloaded again, there are two solutions.
- Firstly, it is recommended to use Linko's dedicated offline downloader to erase. It is recommended to leave a certain margin before switching SWD to GPIO, such as about 100ms, to ensure that the offline downloader can erase the chip and prevent the deadlock. This margin is to ensure a successful offline downloader erasing. A greater margin means a greater probability of the successful one-time erasion.
- Secondly, the application should have a GPIO multiplexing exit mechanism. For example, some other IO invert (usually input), indicates that the SWDIO is required externally, and the software needs to be reconfigured to disable the multiplexing. At this moment, the KEIL function can access the chip via SWD again.

In SSOP24L package and QFN5*5 40L-0.75 package, SWDIO is directly bonded with P0.0 and P2.15, and the corresponding GPIO can be directly enabled. It is recommended that SWDCLK keep unchanged (constant 1 or constant 0) when multiplexing SWDIO

For LKS077E, SWDCLK is bonded with P2.6 and the corresponding GPIO can be directly enabled. If SWDIO and SWDCLK are multiplexed at the same time, considerations for SWDCLK multiplexing are as follows:

- The default state of GPIO multiplexing is disabled, IO are used as SWD. After the hard reset of the chip, the initial state of IOs are SWD. Both IOs of SWD are fixed pull-up inside the chip (the internal pull-up resistor of the chip is about 12K). Please pay attention to the initial IO voltage level if application has specific requirements.
- When GPIO multiplexing is enabled, tools such as KEIL cannot directly access the chip, i.e., the Debug and erase download functions cannot access the chip since SWD are now general GPIO. If the program needs to be downloaded again, there are two solutions.
- Firstly, it is recommended to use Linko's dedicated offline downloader to erase. It is recommended to leave a certain margin before switching SWD to GPIO, such as about 100ms, to ensure that the offline downloader can erase the chip and prevent the deadlock. This margin is to

ensure a successful offline downloader erasing. A greater margin means a greater probability of the successful one-time erasion.

- Secondly, the application should have a GPIO multiplexing exit mechanism. For example, some other IO invert (usually input), indicates that the SWDIO is required externally, and the software needs to be reconfigured to disable the multiplexing. At this moment, the KEIL function can access the chip via SWD again.

When SWDCLK and SWDIO pins are used as GPIO, they should not act at the same time. That is, when SWDCLK multiplexing is enabled and changes, SWDIO can remain at level 0 (similar to time division multiplexing).

For RSTN signal, the default is for the external reset pin of LKS07x chip.

LKS07x allow users to multiplex RSTN as other IOs, and the multiplexed IO is P0.2. The precautions are as follows:

- The default state of reset IO multiplexing is disabled, and the software needs to write 1 to SYS_RST_CFG[5] to multiplex RSTN as GPIO. I.e., the initial state of P0[2] is RSTN. RSTN is provided with a pull-up resistor inside the chip (the internal pull-up resistor of the chip is about 300K). Attention shall be paid when the application has requirements for initial electric level.
- The default state of P0[2] is used as external reset, and the program can only be executed after the RSTN is released. The application needs to ensure that the RSTN has sufficient protection, such as the peripheral circuit with a pull-up resistor. It is better to add a capacitor.
- After RST IO multiplexing is enabled, the external reset is unavailable to the chip. If a hard reset is required, the reset source can only be power-down/watchdog reset.
- The multiplexing of RSTN does not affect the use of KEIL.

Bit [5] in the SYS _ RST _ CFG register controls the switch for multiplexing RSTN and P0.2.

# 26 Ordering Information

Tray Package:

| Package Type | Quantity per disc/tube | Quantity in box | Quantity in case |
|---|---|---|---|
| SOP16/ESOP16L | 3000/ disc | 6000PCS | 48000PCS |
| SSOP24 | 4000/ disc | 8000PCS | 64000PCS |
| SS0P24 | 50/ pipe | 10000PCS | 4000/100000PCS |
| QFN 8*8 | 260/ disc | 2600PCS | 15600PCS |
| QFN 4*4/5*5/6*6 | 490/ disc | 4900PCS | 29400PCS |
| QFN 3*3 | 5000/ disc | 5000PCS | 40000PCS |
| LQFP48/TQFP48 0707 | 250/ disc | 2500PCS | 15000PCS |
| LQFP64 1010 | 160/ disc | 1600PCS | 9600PCS |
| LQFP100 1414 | 90/ disc | 900PCS | 5400PCS |
| TSSOP20/28 | 4000/ disc | 8000PCS | 64000PCS |

Reel Package:

| Package Type | | Quantity per disc/tube | Quantity per box | Quantity boxes per case | Quantity per case |
|---|---|---|---|---|---|
| Braid -13 inches | SOP/ESOP8 | 4000 | 8000 | 8 | 64000 |
| Braid -13 inches | SOP/ESOP16 | 3000 | 6000 | 8 | 48000 |
| Braid -13 inches | SSOP24 | 4000 | 8000 | 8 | 64000 |
| Braid -13 inches | TSSOP20 | 4000 | 8000 | 8 | 64000 |
| Braid -13 inches | D/QFN3*3 | 5000 | 10000 | 8 | 80000 |
| Braid -13 inches | D/QFN4*4 | 5000 | 10000 | 8 | 80000 |
| Braid -13 inches | D/QFN5*5 | 5000 | 10000 | 8 | 80000 |
| Pipe | SOP16 | 50 | 10000 | 10 | 100000 |
| Pipe | SOP14/SSOP24 | 50 | 10000 | 10 | 100000 |
| Pipe | TSSOP24 | 54 | 6480 | 6 | 38880 |

# 27 Version history

Table27-1Document version history

| Time | Version No. | Description |
|---|---|---|
| 2026.06.11 | 1.36 | Remove Model 072KBT8 from the selection list |
| 2026.06.10 | 1.35 | Revise the description of CAN in the selection table |
| 2026.03.09 | 1.34 | Revise the CMP trip voltage parameters |
| 2026.01.27 | 1.33 | Electrical Parameters – Other Models Omitted |
| 2026.01.26 | 1.32 | Add the configuration description block diagram for the DAC module. |
| 2026.01.20 | 1.31 | Add ADC configuration flowchart, and delete the description that the CAN requires an external crystal oscillator. |
| 2026.01.12 | 1.30 | Revise the pin description of KBT8 |
| 2026.01.08 | 1.29 | Remove non-matching model types from the selection table. |
| 2025.12.28 | 1.28 | Revise the MCPWM module description to: Two chopper modules, with each group sharing one dead-time configuration. |
| 2025.12.24 | 1.27 | Retain only LQFP48 for the 07 series packaging. |
| 2025.11.03 | 1.26 | Revised OPA Module Common-Mode Level |
| 2025.09.16 | 1.25 | Add SPI module |
| 2025.09.04 | 1.24 | CBT8/C8T8 add LQFP48 package diagram and dimensions |
| 2025.08.22 | 1.23 | Update naming rules |
| 2025.08.21 | 1.22 | CBT8 and C8T8 packages changed to LQFP48 |
| 2025.08.14 | 1.21 | CBT8 and C8T8 add LQFP package |
| 2025.08.06 | 1.20 | KBT8 Update Pin Information |
| 2025.07.21 | 1.19 | Delete the Flash section: erase/program one sector while accessing another |
| 2025.04.02 | 1.18 | Modify the pull-up resistor |
| 2025.03.26 | 1.17 | Add 32kb EEPROM，P0.9 connected to SCL，P0.10 connected to SDA |
| 2025.01.02 | 1.16 | Update the offset voltage of the CMP |
| 2024.09.29 | 1.15 | The belly Pad grounding of a QFN package is defined as Pin0 |
| 2024.08.28 | 1.14 | Modify the mapping between MCPWM and GPIO of 072KBT8 |
| 2024.08.14 | 1.13 | Add LKS32MC072KBT8 |
| 2024.08.04 | 1.12 | Order package information updates to confirm package information by package type and package form |
| 2024.03.12 | 1.11 | Add LKS32MC073HBQ8 |
| 2023.12.20 | 1.1 | Update 072 FLASH size |
| 2023.11.20 | 1.09 | Add description of OPA offset |
| 2023.10.22 | 1.08 | Modify the device selection table |
| 2023.09.25 | 1.07 | Update welding temperature, modify non-volatile memory Sector erase description |
| 2023.08.23 | 1.06 | Update 072/077 FLASH size |
| 2023.07.27 | 1.05 | Modify/updated a new model 07x 6N in the device selection table |
| 2023.07.04 | 1.04 | LKS32MC071C8T8 removes CAN function,modify the opa output sig- |

| | | |
|---|---|---|
| | | nal range, power supply range,sleep power consumption and Vcm |
| 2023.05.16 | 1.03 | Add LKS32MC071C8T8 |
| 2023.05.07 | 1.02 | Update the number of times the flash can be erased repeatedly |
| 2023.04.07 | 1.01 | Update package description |
| 2023.03.16 | 1.0 | Initial version |

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