Linko Semiconductor Co., Ltd.

LKS32MC07X with built-in 3P3N driver Datasheet

1 Overview

1.1 Functions

LKS32MC074F/076F is a 32-bit MCU targeting motor control applications. With all modules required for common motor control systems and three-phase P/N MOS gate driver, it can directly drive three-channel P/N MOS power device.

- **Features**
  - 96MHz 32-bit Cortex-M0 core
  - Customized instruction set DSP for motor control
  - Ultra low power sleep mode
  - Three-phase full-bridge bootstrap gate driver
  - Industrial temperature range
  - High ESD and group pulse reliability
- **Memory**
  - Built-in flash including 64kB/128kB main area and 1.5kB NVR
  - Endurance: 100,000 Cycles(min)
  - Data retention: more than 100 years under room temperature 25 ℃
  - Single byte program: 7.5us(max), Sector erase: 5ms(max)
  - Sector size 512bytes, supporting Sector erase/program
  - Flash data anti-theft by programming the last word of flash to any words other than 0xFFFFFFFF
- **Operating Conditions**
  - 7.5~32V (Maximum: 40V), single power supply, with an integrated internal 5V LDO for partial power supply for internal MCU of chip
  - Operating Conditions: -40~105℃
- **Clock**
  - 8MHz built-in high-precision RC oscillator, with an accuracy of ± 1% at -40 ~ 105 ℃
  - 32KHz built-in low-speed clock for low-power mode
  - Operating on an external 8MHz crystal is available
  - Internal PLL up to 96 MHz
- **Peripheral module**
  - Two UARTs
  - Two 16-bit standard timers (TIM), support capture and edge-aligned PWM function
  - Two 32-bit standard timers (TIM), support capture and edge-aligned PWM function; support orthogonal code input, CW/CCW input, and pulse&symbol input
  - Motor control PWM module, supports 12 channels/6 pairs of PWM waveform output, inde-

pendent dead-band control

- Hall signal interface with speed measurement and debouncing function
- Hardware watchdog
- 4 Groups of 16bit GPIO at the most. 8 GPIOs could be used as wake-up source,15 GPIOs could be used as external IRQ source

- **Simulation module**
  - Two 12bit SAR ADC, simultaneous double sampling, 3Msps sampling and conversion rate, and each sampling circuit supports up to 16 channels, including 4 OPA outputs and 10 ex-ternal ADC channels for a total of 14 optional ADC channel signals
  - Four operational amplifiers. Differential PGA mode is available.
  - Three comparators. Hysteresis mode is available.
  - Two 12bit digital-to-analog converter (DAC)
  - ± 2 ℃ built-in temperature sensor
  - 1.2V 0.8% built-in linear regulator
  - Low-power LDO and power monitoring circuit
  - RC oscillator with high precision and low temperature drift
  - Crystal oscillator circuits
  - Integrated 32kHz+4MHz RC
  - Integrated 96MHz PLL

1.2 Performance advantages

- High reliability, high integration level, small package size, saving BOM cost;
- Integrated 4 channels high-speed OPAs and 3 channels comparators, meeting the needs of different system topology like single resistance/double resistance/three resistance current sampling;
- High-speed OPA is integrated with over-voltage protection circuit, which allows high-voltage common-mode signals to be input, which could support direct current sampling of MOSFET resistance with the simplest circuit topology.
- Via a proprietary technique, ADC and high-speed OPA could cooperate well, making them able to handle a wider current dynamic range, while ensuring the sampling precision of high-speed small current and low-speed high current;
- The control circuit is simple and efficient, with strong anti-interference ability, stable and reliable;
- Single power 7.5~32V supply, integrated 5V LDO internally;
- Three-phase full-bridge bootstrap gate driver is integrated
- Supports IEC/UL60730 functional safety certification

Applicable to control systems such as inductive BLDC/non-inductive BLDC/inductive FOC/non-inductive FOC and stepper motors, permanent magnet synchronous and asynchronous motors.

1.3 Naming Conventions

LKS32 MC 070 D 2 M 6 S 8 B (XX)

Device series

LKS32	= 32bit MCU
LKS5	= Gate Driver Products
LKS6	= Power IC Product

Product type

MC	= Motor Control Applications
AT	= Automobile Applications
RV	= RISC-V for Motor Control

Device sub family

070/071/075	= 2.5~5.5V,2 ADC,4 PGA,DSP
070FL/071DO/074D/DO	= 2.5~5.5V,2 ADC,4 PGA,DSP,6N Driver
076/076F	= 2.5~5.5V,2 ADC,3 PGA,DSP,6N Driver
072	= 2.5~5.5V,2 ADC,3 PGA
077	= 2.5~5.5V,2 ADC,2 PGA
077E	= 7.5~28V, 2 ADC,2 PGA,3P3N Driver

Gate Driver Functions

D	= 3P3N Gate Driver
E/DL	= 3P3N + 5V LDO
S/F	= 6N Gate Driver
SL/FL	= 6N + 5V LDO
K	= High V 6N Gate Driver
O/L5	= 5V LDO/DCDC
L3	= 3.3V/3V LDO
N	= DCDC
P	= 3P3N/4P4N DrMOS
Q	= 6N/8N DrMOS
PL3	= 3P3N DrMOS + 3.3VLDO
PL5	= 3P3N DrMOS + 5VLDO
QL	= 6N DrMOS + LDO
X	= PHY
XL	= PHY + LDO

PKG/Driver Ver

2	= 2nd Ver
S	= S 側面上锡

Pin count

L	=16 pins
H	= 20 pins
M	= 24 pins
Y	=28 pins
K	= 32 pins
F	= 40 pins
G	= 42 pins
U	= 44 pins
C	= 48 pins
N	= 52 pins
S	= 54pins
E	= 60 pins
R	= 64 pins
P	= 80 pins
V	=100 pins
Q	=128 pins
Z	=144 pins

Code size

4	= 16Kbyte Flash Memory
6	= 32Kbyte Flash Memory
8	= 64Kbyte Flash Memory
B	=128Kbyte Flash Memory
C	=256Kbyte Flash Memory
D	=384Kbyte Flash Memory
E	=512Kbyte Flash Memory

Package

P	= TSSOP
T	= TQFP/LQFP
Q	= QFN
S	= SSOP
H	= BGA

Temperature range

6	= -40~85°
8	= -40~105°
9	= -40~125°

MCU Ver

B	= B ver

Options

TR	= Tape and reel packing
P	= ES

Fig.1-1 Naming Conventions of Linko Components

1.4 Resource Diagram

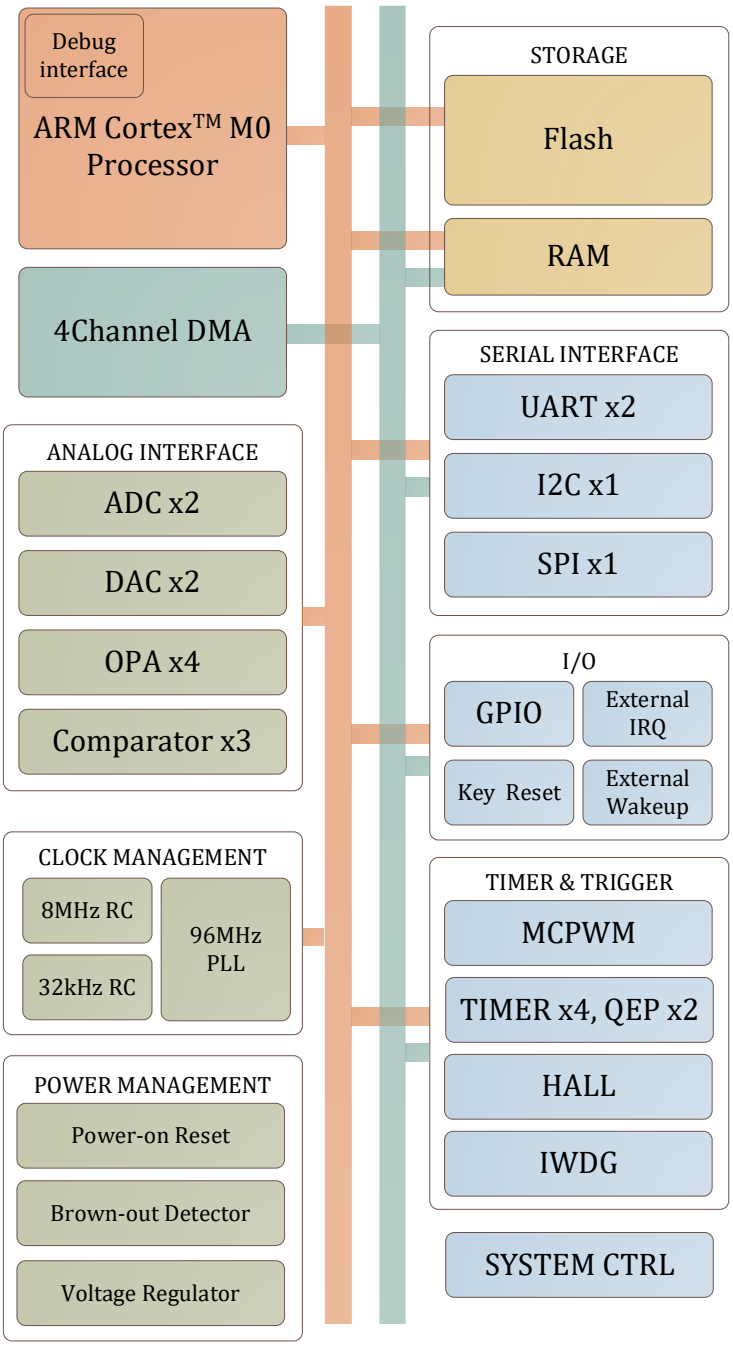
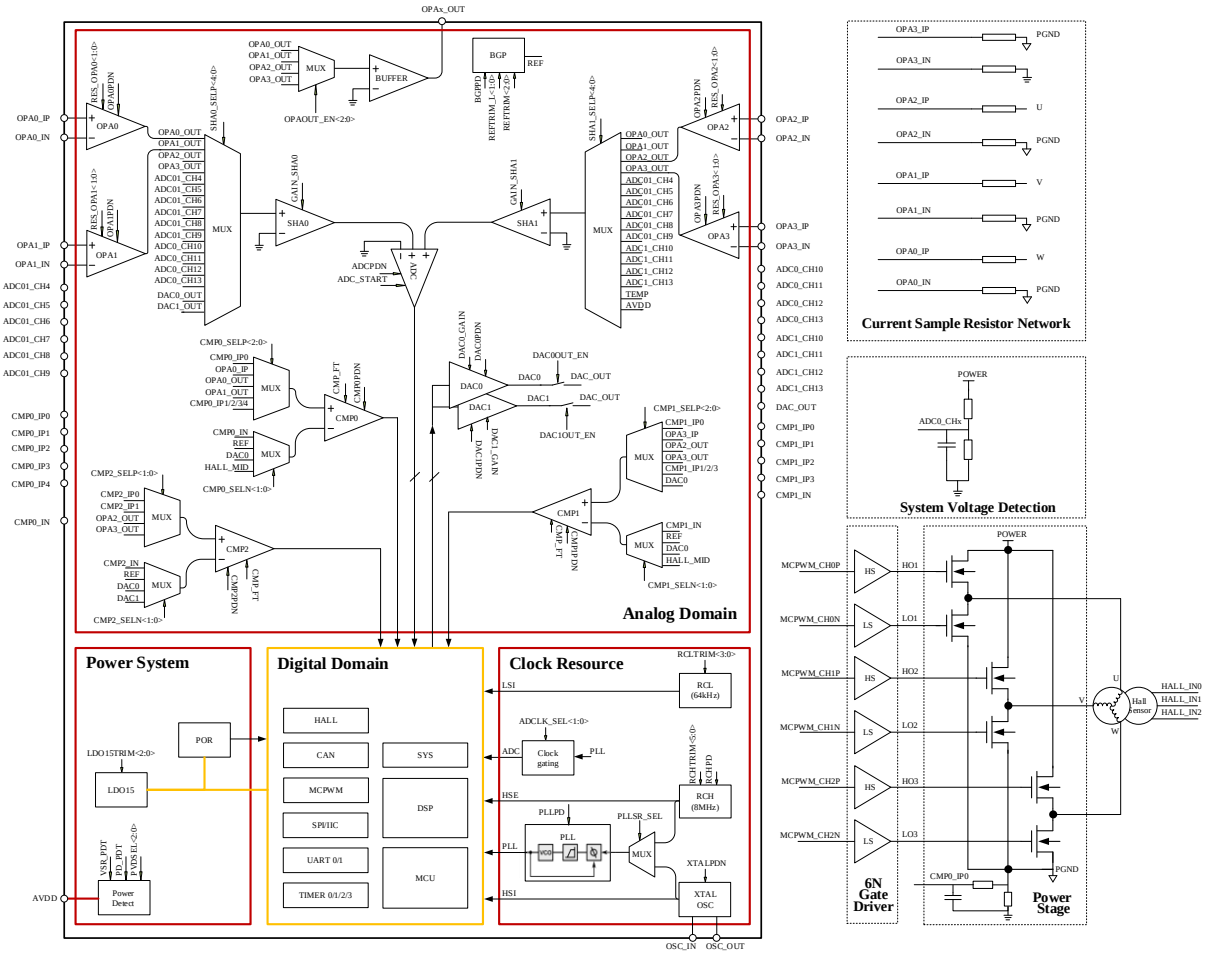


Fig. 1-2 LKS32MC07x Resource Diagram

1.5 FOC System Example



* ADC 01 _ CH4 ~ ADC 01 _ CH9 are common channels for ADC0 and ADC 1

Fig.1-3 LKS32MC077EM6S8 Simplified Schematic of FOC System

2 Device selection table

Table 2-1 LKS07x Series Device Selection Table

	Frequency (MHz)	Flash (kB)	RAM (kB)	ADC ch.	DAC	Comparator	Comparator ch.	OPA	HALL	SPI	IIC	UART	CAN	Temp. Sensor	PLL	QEP	Gate driver	Gate Driver current (A)	Pre-drive supply (V)	Gate floating voltage (V)	Others	Package
LKS32MC077EM8S8	96	64	12	6	12BITx2	3	7	2	3	1	1	2		Yes	Yes	Yes	3P3N	+0.05/-0.3	7~32		5V LDO	SSOP24L

3 Pin Assignment

3.1 Pin Assignment and Pin Function Description

3.1.1 Special instructions

The red pin in the pin assignment figures below has built-in pull-up resistors:
RSTN has a 100kΩbuilt-in pull-up resistor, which is enabled automatically after power-up.
SWDIO/SWCLK has a 10kΩ built-in pull-up resistor, which is enabled automatically after power-up.
The remaining red pins have 10kΩ built-in pull-up resistors, which could be software-enabled.

UARTx_TX(RX): UART TX and RX support interchange. When the second function of GPIO is selected as UART, and GPIO_PIE is input enabled, it can be used as UART_RX; when GPIO_POE is enabled, it can be used as UART_TX. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

SPI_DI(DO): The DI and DO of SPI can also be interchanged. When the second function of GPIO is SPI, and GPIO_PIE is input enable, it can be used as SPI_DI; when GPIO_POE is output enable, it can be used as SPI_DO. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

3.1.2 LKS32MC077EM8S8

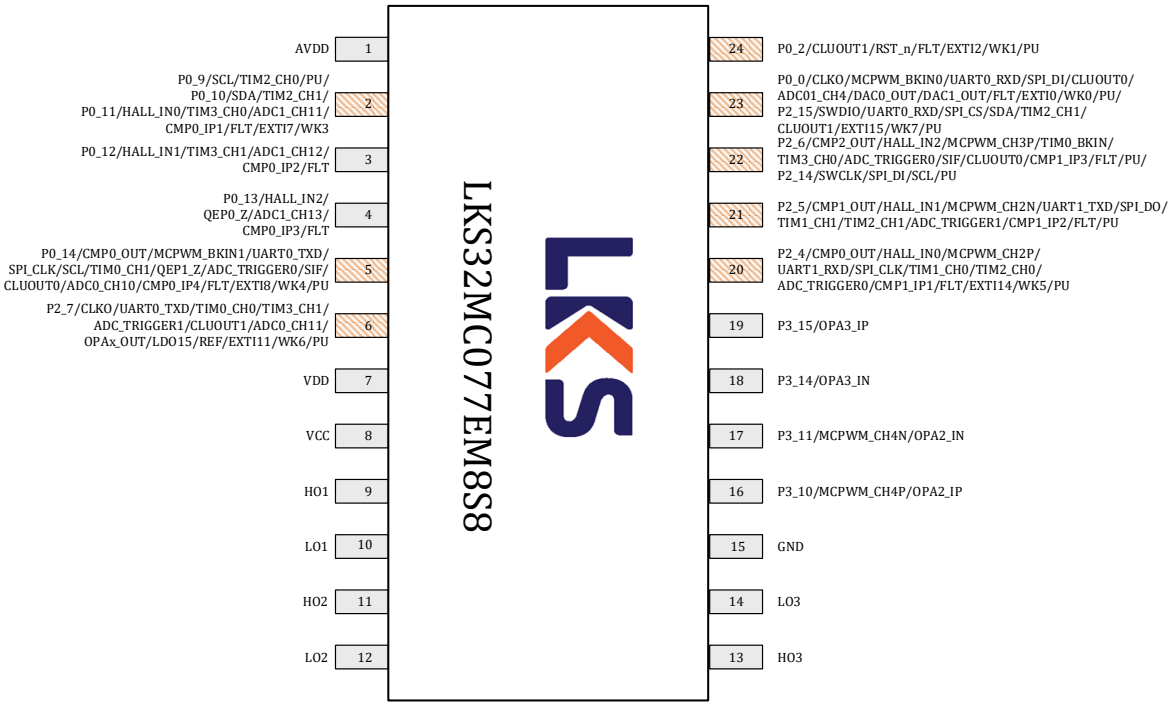


Fig.3-1 LKS32MC077EM8S8 Pin Assignment

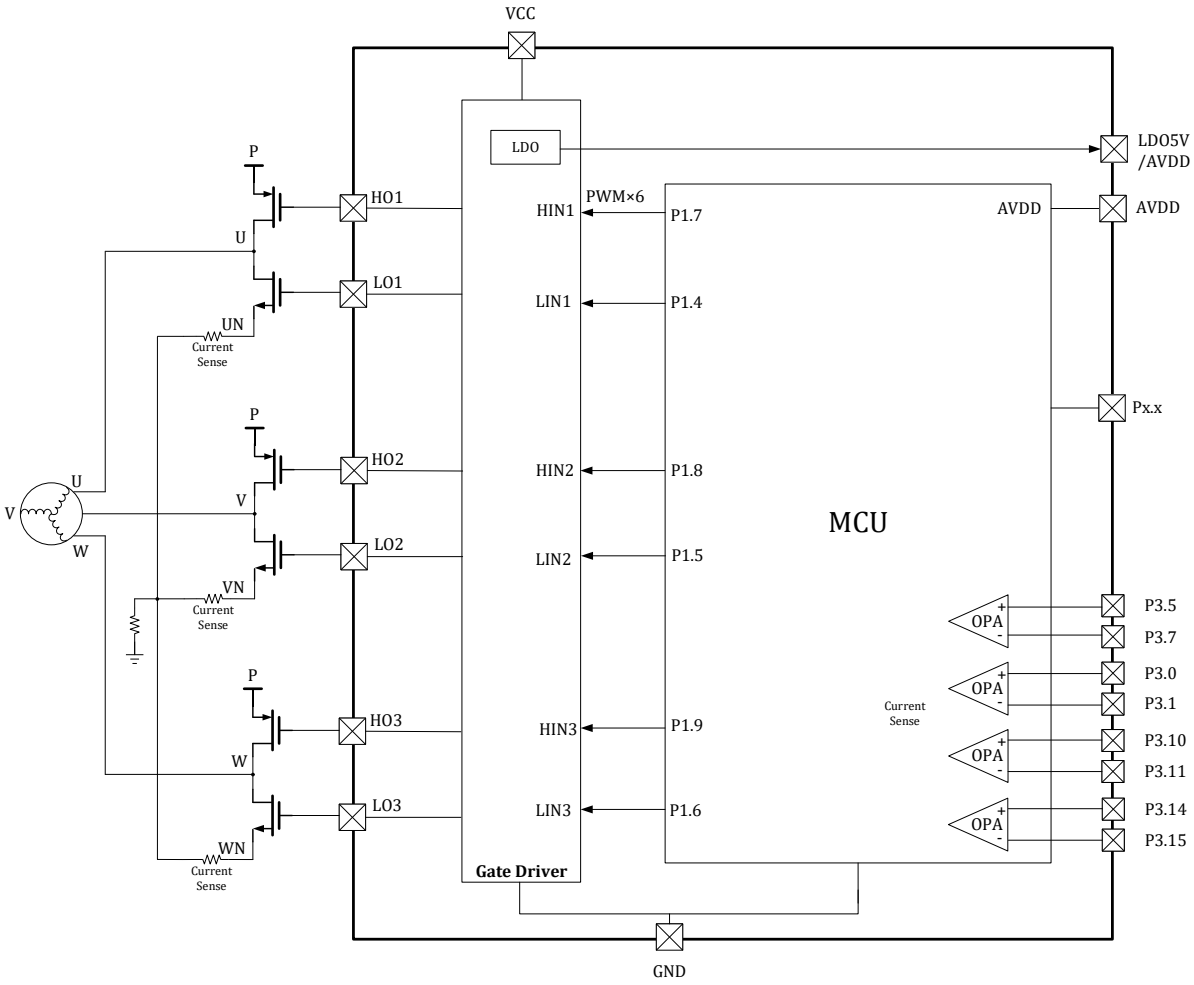


Fig.3-2 LKS32MC077EM8S8 Schematic diagram of inner driver connection

Notice: Do not pull up the LDO before the VCC is powered on. Otherwise, the LDO may fail to start after the VCC is powered on.

Table 3-1 LKS32MC077EM8S8 Pin Function Description

1	AVDD	Chip power supply, power supply range 2.5 ~ 5.5V
2	P0_9	P0.9
	SCL	I2C clock
	TIM2_CH0	Timer2 channel 0
	PU	Built-in 10kΩ pull-up resistor, software can be turned off
	P0_10	P0.10
	SDA	I2C data
	TIM2_CH1	Timer2 channel 1
	P0_11	P0.11
	HALL_IN0	HALL interface input 0
	TIM3_CH0	Timer3 channel 0
	ADC1_CH11	ADC1 Channel 11
	CMP0_IP1	Comparator 0 positive input 1
	FLT	IO filtering
	EXTI7	External GPIO Interrupt Signal 7

	WK3	External wake-up signal 3
3	P0_12	P0.12
	HALL_IN1	HALL interface input 1
	TIM3_CH1	Timer3 channel 1
	ADC1_CH12	ADC1 Channel 12
	CMP0_IP2	Comparator 0 positive input 2
	FLT	IO filtering
4	P0_13	P0.13
	HALL_IN2	HALL interface input 2
	QEP0_Z	QEP0 Encoder Phase Z
	ADC1_CH13	ADC1 Channel 13
	CMP0_IP3	Comparator 0 positive input 3
	FLT	IO filtering
5	P0_14	P0.14
	CMP0_OUT	Comparator 0 Output
	MCPWM_BKIN1	PWM Shutdown Input Signal 1
	UART0_TXD	Serial port 0 send (receive)
	SPI_CLK	SPI clock
	SCL	I2C clock
	TIM0_CH1	Timer0 channel 1
	QEP1_Z	Phase Z of QEP1 encoder
	ADC_TRIGGER0	ADC0 trigger signal output (for debugging)
	SIF	Single line communication
	CLUOUT0	CLU0 output
	ADC0_CH10	ADC0 Channel 10
	CMP0_IP4	Comparator 0 positive input 4
	FLT	IO filtering
	EXTI8	External GPIO Interrupt Signal 8
	WK4	External wake-up signal 4
	PU	Built-in 10kΩ pull-up resistor, software switchable
6	P2_7	P2.7
	CLKO	Clock output (for debugging)
	UART0_TXD	Serial port 0 send (receive)
	TIM0_CH0	Timer0 channel 0
	TIM3_CH1	Timer3 channel 1
	ADC_TRIGGER1	ADC1 trigger signal output (for debugging)
	CLUOUT1	CLU1 output
	ADC0_CH11	ADC0 Channel 11
	OPAx_OUT	Op Amp Output
	LDO15	1.5V LDO Output
	REF	Reference Voltage
	EXTI11	External GPIO Interrupt Signal 11
	WK6	External wake-up signal 6

	PU	Built-in 10kΩ pull-up resistor, software can be turned off
7	VDD	Supply voltage of devices in the chip， 5V LDO output
8	VCC	Full-bridge drive power supply
9	HO1	Phase A high-side output is controlled by MCU P1.7, and the polarity of HO1 is the same as P1.7, that is, when P1.7 = 1, HO1 = 1. PWM _ SWAP = 1 needs to be set.
10	LO1	Phase A low-side output, controlled by MCU P1.4, LO1 polarity is the same as P1.4, that is, when P1.4 = 1, LO1 = 1. PWM _ SWAP = 1 needs to be set.
11	HO2	Phase B high-side output is controlled by MCU P1.8. The polarity of HO2 is the same as P1.8. That is, when P1.8 = 1, HO2 = 1. PWM _ SWAP = 1 needs to be set.
12	LO2	Phase B low-side output, controlled by MCU P1.5, LO2 polarity is the same as P1.5, that is, when P1.5 = 1, LO2 = 1. PWM _ SWAP = 1 needs to be set.
13	HO3	Phase C high-side output is controlled by MCU P1.9. The polarity of HO3 is the same as P1.9, that is, when P1.9 = 1, HO3 = 1. PWM _ SWAP = 1 needs to be set.
14	LO3	Phase C low-side output, controlled by MCU P1.6, LO3 polarity is the same as P1.6, that is, when P1.6 = 1, LO3 = 1. PWM _ SWAP = 1 needs to be set.
15	GND	Chip ground. It is strongly recommended that multiple ground pins be grounded uniformly on the PCB.
16	P3_10	P3.10
	MCPWM_CH4P	PWM Channel 4 High Side
	OPA2_IP	Positive input of operational amplifier 2
17	P3_11	P3.11
	MCPWM_CH4N	PWM Channel 4 Low Side
	OPA2_IN	Op Amp 2 Negative Input
18	P3_14	P3.14
	OPA3_IN	Op Amp 3 Negative Input
19	P3_15	P3.15
	OPA3_IP	Positive input of operational amplifier 3
20	P2_4	P2.4
	CMP0_OUT	Comparator 0 Output
	HALL_IN0	HALL interface input 0
	MCPWM_CH2P	PWM Channel 2 High Side
	UART1_RXD	Serial port 1 receive (send)
	SPI_CLK	SPI clock
	TIM1_CH0	Timer1 channel 0
	TIM2_CH0	Timer2 channel 0
	ADC_TRIGGER0	ADC0 trigger signal output (for debugging)
	CMP1_IP1	Comparator 1 positive input 1
	FLT	IO filtering
	EXTI14	External GPIO Interrupt Signal 14
	WK5	External wake-up signal 5
	PU	Built-in 10kΩ pull-up resistor, software switchable
21	P2_5	P2.5
	CMP1_OUT	Comparator 1 Output

	HALL_IN1	HALL interface input 1
	MCPWM_CH2N	PWM Channel 2 Low Side
	UART1_TXD	Serial port 1 send (receive)
	SPI_DO	SPI Data Output (Input)
	TIM1_CH1	Timer1 channel 1
	TIM2_CH1	Timer2 channel 1
	ADC_TRIGGER1	ADC1 trigger signal output (for debugging)
	CMP1_IP2	Comparator 1 positive input 2
	FLT	IO filtering
	PU	Built-in 10kΩ pull-up resistor, software switchable
22	P2_6	P2.6
	CMP2_OUT	Comparator 2 Output
	HALL_IN2	HALL interface input 2
	MCPWM_CH3P	PWM Channel 3 High Side
	TIM0_BKIN	TIMER0_FAIL com from GPIO
	TIM3_CH0	Timer3 channel 0
	ADC_TRIGGER0	ADC0 trigger signal output (for debugging)
	SIF	Single line communication
	CLUOUT0	CLU0 output
	CMP1_IP3	Comparator 1 positive input 3
	FLT	IO filtering
	P2_14	P2.14
	SWCLK	SWD clock
	SPI_DI	SPI Data In (Out)
	SCL	I2C clock
	PU	Built-in 10kΩ pull-up resistor, software switchable
23	P0_0	P0.0
	CLKO	Clock output (for debugging)
	MCPWM_BKIN0	PWM shutdown input signal 0
	UART0_RXD	Serial port 0 receive (send)
	SPI_DI	SPI Data In (Out)
	CLUOUT0	CLU0 output
	ADC0_CH4	ADC 0/ADC1 Channel 4
	DAC01_OUT	DAC0 output
	DAC1_OUT	DAC1 Output
	FLT	IO filtering
	EXTI0	External GPIO Interrupt Signal 0
	WK0	External wake-up signal 0
	PU	Built-in 10kΩ pull-up resistor, software switchable
	P2_15	P2.15
	SWDIO	SWD data
	UART0_RXD	Serial port 0 receive (send)
	SPI_CS	SPI chip select

	SDA	I2C data
	TIM2_CH1	Timer2 channel 1
	CLUOUT1	CLU1 output
	EXTI15	External GPIO Interrupt 15
	WK7	External wake-up signal 7
	PU	Built-in 10kΩ pull-up resistor, software switchable
24	P0_2	P0.2
	CLUOUT1	CLU1 output
	RST_n	Reset pin, P0.2 used as RSTN by default. It is recommended to connect a 10 nF to 100 nF capacitor to ground and place a 10 K to 20 K pull-up resistor between RSTN and AVDD. If there is an external pull-up resistor, the capacitance of RSTN should be 100 nF. P0.2 can be switched as a GPIO, which turns off the 10 kΩ pull-up resistor.
	FLT	IO filtering
	EXTI2	External GPIO Interrupt Signal 2
	WK1	External wake-up signal 1
	PU	Built-in 10kΩ pull-up resistor, software switchable

3.2 Description of Pin Multiplex Function

Table 3-2 LKS32MC07X Pin Function Selection

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF0
P0.0	CLKO		MCPWM_BKIN0	UART0_RXD	SPI_DI							CLUOUT0	ADC01_CH4/ DAC0_OUT/ DAC1_OUT
P0.1													ADC01_CH6
P0.2												CLUOUT1	
P0.3			MCPWM_CH4P			SCL		TIM2_CH0					ADC01_CH7
P0.4			MCPWM_CH4N			SDA		TIM2_CH1					ADC01_CH8
P0.5		HALL_IN0	MCPWM_CH5P					QEP0_Z					ADC01_CH9
P0.6		HALL_IN1	MCPWM_CH5N	UART1_RXD		SCL	TIM1_CH0			CAN_RX			CMP2_IN
P0.7		HALL_IN2	MCPWM_BKIN1	UART1_TXD		SDA	TIM1_CH1			CAN_TX			CMP2_IP0
P0.8													
P0.9						SCL		TIM2_CH0					
P0.10						SDA		TIM2_CH1					
P0.11		HALL_IN0						TIM3_CH0					ADC1_CH11/ CMP0_IP1
P0.12		HALL_IN1						TIM3_CH1		CAN_RX			ADC1_CH12/ CMP0_IP2
P0.13		HALL_IN2						QEP0_Z		CAN_TX			ADC1_CH13/ CMP0_IP3
P0.14	CMP0_OUT		MCPWM_BKIN1	UART0_TXD	SPI_CLK	SCL	TIM0_CH1	QEP1_Z	ADC_TRIGGER0		SIF	CLUOUT0	ADC0_CH10/ CMP0_IP4
P0.15	CMP2_OUT		MCPWM_CH0P	UART0_RXD	SPI_DO	SDA	TIM0_CH0		ADC_TRIGGER1				CMP0_IN

Table 3-3 LKS32MC07X Pin Function Selection (continued)

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF0
P1.0			MCPWM_CH0N	UART0_TXD	SPI_DI		TIM0_BKIN						
P1.1					SPI_CS								
P1.2								TIM3_CH0					
P1.3								TIM3_CH1					ADC01_CH5
P1.4			MCPWM_CH0P					QEP0_Z					
P1.5			MCPWM_CH0N										
P1.6			MCPWM_CH1P										
P1.7			MCPWM_CH1N										
P1.8			MCPWM_CH2P										
P1.9			MCPWM_CH2N										
P1.10			MCPWM_CH3P	UART0_RXD		SCL	TIM0_CH0		ADC_TRIGGER0				ADC0_CH13
P1.11			MCPWM_CH3N	UART0_TXD		SDA	TIM0_CH1		ADC_TRIGGER1		SIF	CLUOUT2	
P1.12													
P1.13			MCPWM_CH5P		SPI_CLK		TIM0_CH0						
P1.14			MCPWM_CH5N		SPI_DO		TIM0_CH1						
P1.15			MCPWM_CH4P		SPI_DI			TIM2_CH0					

Table 3-4 LKS32MC07X Pin Function Selection (continued)

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF0
P2.0			MCPWM_CH4N		SPI_CS			TIM2_CH1					
P2.1					SPI_CLK								ADC1_CH10/ CMP1_IP0
P2.2								QEP1_Z					CMP1_IN
P2.3	CMP1_OUT		MCPWM_BKIN0		SPI_CS		TIM0_CH1	QEP0_Z				CLUOUT3	
P2.4	CMP0_OUT	HALL_IN0	MCPWM_CH2P	UART1_RXD	SPI_CLK		TIM1_CH0	TIM2_CH0	ADC_TRIGGER0	CAN_RX			CMP1_IP1
P2.5	CMP1_OUT	HALL_IN1	MCPWM_CH2N	UART1_TXD	SPI_DO		TIM1_CH1	TIM2_CH1	ADC_TRIGGER1	CAN_TX			CMP1_IP2
P2.6	CMP2_OUT	HALL_IN2	MCPWM_CH3P				TIM0_BKIN	TIM3_CH0	ADC_TRIGGER0		SIF	CLUOUT0	CMP1_IP3
P2.7	CLKO			UART0_TXD			TIM0_CH0	TIM3_CH1	ADC_TRIGGER1	CAN_TX		CLUOUT1	ADC0_CH11/ OPAx_OUT/ LDO15/REF
P2.8				UART1_RXD	SPI_DO			TIM3_CH0					OSC_IN
P2.9			MCPWM_CH5P		SPI_DI	SCL							ADC0_CH12/ CMP0_IP0
P2.10			MCPWM_CH5N		SPI_DO	SDA							
P2.11			MCPWM_CH1P					TIM2_CH0					CMP2_IP1
P2.12			MCPWM_CH1N		SPI_CS			TIM2_CH1	ADC_TRIGGER0			CLUOUT3	
P2.13			MCPWM_CH3N	UART0_TXD	SPI_DO	SCL		TIM3_CH1					
P2.14	SWCLK				SPI_DI	SCL							
P2.15	SWDIO			UART0_RXD	SPI_CS	SDA		TIM2_CH1				CLUOUT1	

Table 3-5 LKS32MC07X Pin Function Selection (continued)

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF0
P3.0													OPA1_IP
P3.1													OPA1_IN
P3.2			MCPWM_CH3P									CLUOUT2	
P3.3													
P3.4			MCPWM_CH3N										
P3.5													OPA0_IP
P3.6													
P3.7													OPA0_IN
P3.8													
P3.9				UART1_TXD				TIM3_CH1					OSC_OUT
P3.10			MCPWM_CH4P										OPA2_IP
P3.11			MCPWM_CH4N										OPA2_IN
P3.12													
P3.13													
P3.14													OPA3_IN
P3.15													OPA3_IP

4 Package size

SSOP24L Profile Quad Flat Package:

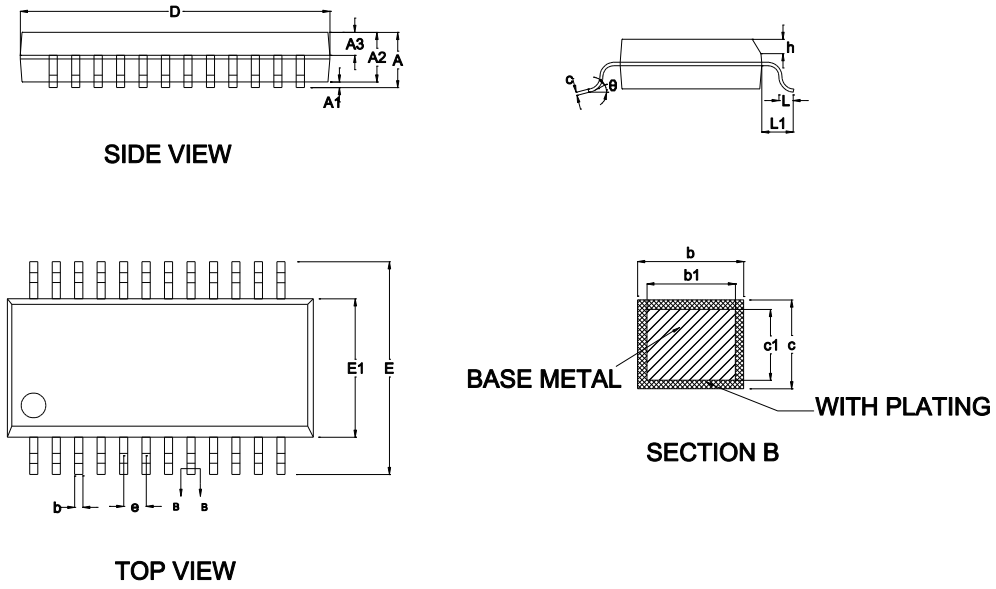


Fig.4-1 LKS32MC077EM6S8 Package Diagram

Table 4-1 LKS32MC077EM6S8 Package Dimension

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

5 Analog Characteristics

Table 5-1 LKS32MC077EM6S8 analog characteristics

Parameter	Min.	Typ.	Max.	Unit	Explain
Analog-to-digital converter (ADC)					
Power Supply	3.3	5	5.5	V	ADC use 2.4V internal reference
	2.8	5	5.5	V	ADC use 1.2V internal reference
Sampling rate		3		MHz	fadc/16
Differential Input Signal Range	-5.0 +0.144		+5.0 -0.144	V	When ADCx_GAIN = 1; REF=2.4V;
	-3.6 +0.072		+3.6 -0.072	V	When ADCx_GAIN = 0; REF=2.4V;
Single-ended Input Signal Range	-0.3		AVDD +0.3	V	Limited by the input voltage of the IO port
The differential signal is usually the signal output from the OPA inside the chip to the ADC; Single-ended signals are typically sampled externally via an I0 input: The ADC should measure the signal amplitude no more than ±98% of the full scale, regardless of the internal/external reference used. In particular, when using an external reference, it is recommended that the sampling conductor not exceed 90% of the scale.					
DC offset		5	10	mV	Correctable
Effective number of bits (ENOB)	10.5	11		bit	
INL		2	3	LSB	
DNL		1	2	LSB	
SNR	63	66		dB	
Input Resistance	100k			Ohm	
Input Capacitance		10		pF	
Reference Voltage (REF)					
Power Supply	2.2	5	5.5	V	
Output Deviation	-9		9	mV	
Rejection Ratio of Power Supply		70		dB	
Temperature Coefficient		20		ppm/°C	
Output Voltage		1.2		V	
Digital-to-Analog Converter (DAC)					
Power Supply	2.2	5	5.5	V	
Load Resistance	5k			Ohm	Output BUFFER is on
Load capacitance			50p	F	
Output voltage range	0.05		AVDD-0.1	V	
Conversion speed			1M	Hz	
DNL		1	2	LSB	

Parameter	Min.	Typ.	Max.	Unit		Explain
INL		2	4	LSB		
OFFSET		5	10	mV		
SNR	57	60	66	dB		
Operational Amplifier (OPA)						
Power Supply	2.8	5	5.5	V		
Bandwidth		10	20	MHz		
Load Resistance	20k			Ohm		
Load Capacitance			5p	F		
Input Common Mode Voltage Range (VICM)	0		AVDD	V		
Output Signal Range	0		2Vcm	V		Under minimum load resistance
Common Mode Voltage (Vcm)	1.45	1.8	2.2	V	32 times	Measurement condition: normal temperature. Operational amplifier swing=2 × min(AVDD-Vcm, Vcm). It is recommended that the application using OPA single output should be powered on to measure Vcm and make software subtraction correction. For more analysis, please refer to the official website application note "ANN009 - Differences between Operational Amplifier Differential and Single Operating Mode".
	1.5	1.8	2.2	V	16 times	
	1.55	1.8	2.2	V	8 times	
	1.6	1.8	2.2	V	4 times	
OFFSET		10	15.0	mV		32 times
		10	16.5	mV		16 times
		10	18.5	mV		8 times
		10	20.5	mV		4 times
This OFFSET is the equivalent differential input deviation obtained when the OPA differential input is short-circuited and OPA OUT is measured from 0 level. The output deviation of OPA is OPA magnification x OFFSET. The Flash NVR area records the OPA offset for factory tests.						
Common Mode Rejection Ratio (CMRR)		80		dB		
Power Supply Rejection Ratio (PSRR)		80		dB		
Load Current			500	uA		
Slew Rate		5		V/us		
Phase Margin (PM)		60		Degree		

Parameter	Min.	Typ.	Max.	Unit	Explain
Comparator (CMP)					
Power Supply	2.2	5	5.5	V	
Input Signal Range	0		AVDD	V	
OFFSET	-36	-10	12	mV	0 mV hysteresis, CMP output transitions from low to high
	-36	-10	12	mV	0 mV hysteresis, CMP output transitions from high to low
	-14.5	-10	33.5	mV	20 mV hysteresis, CMP output transitions from low to high
	-14.5	11.5	33.5	mV	20 mV hysteresis, CMP output transitions from high to low
Delay		50		nS	Default power consumption
		200		nS	Low power consumption
Hysteresis		20		mV	HYS='0'
		0		mV	HYS='1'

Analog register table description:

The names of the analog registers are SYS_AFE_REG0 to SYS_AFE_REG6, corresponding to addresses 0x4000 0010 to 0x4000_0028. Address 0x4000_001C to 0x4000_0028 are the calibration registers of each analog module. These registers will fill their respective calibration values into the Flash info area before leaving the factory, and will be automatically loaded to the SYS _ AFE _ REG3 to SYS _ AFE _ REG6 after power-on. In general, the user should not configure or change these values. If fine-tuning is required, please read the original settings first, and then adjust based on those values.

Addresses space of 0x4000_0000 to 0x4000_0018 are registers open to users. The blank registers must be configured to 0 (these registers will be reset to 0 after power on). Other registers could be configured in situations.

6 Electrical performance parameters

Table 6-1 LKS32MC077EM6S8 electrical absolute characteristics

Parameter	Min.	Max.	Unit	Explain
MCU Power Supply Voltage (AVDD)	-0.3	+6.0	V	
Gate Driver Power Supply Voltage (VCC)	-0.3	+40.0	V	
5V LDO output current		40	mA	
Operating temperature	-40	+105	˚C	
Storage temperature	-40	+150	˚C	
Junction temperature	-	125	℃	
Pin temperature (soldering for 10 seconds)	-	260	℃	

Table 6-2 LKS32MC077EM6S8 Recommended working condition parameters

Parameter	Mini.	Typ.	Max.	Unit	Explain
MCU Power Supply Voltage (AVDD)	2.5	5	5.5	V	
Analog Power Supply Voltage ($AVDD_A$)	3.3	5	5.5	V	REF2VDD = 0, ADC selects 2.4 V internal reference
	2.8	5	5.5	V	REF2VDD = 1, ADC selects AVDD as reference
Gate Driver Power supply voltage (VCC)	7.5		32	V	When VCC＜7.5V, 3P3N Gate driver will be shut down while MCU could still work normally

Table 6-3 LKS32MC077EM6S8 ESD Parameters

Item	Pin	Minimal	Max	Unit
ESD Test (HBM)	MCU(Pin 1-6,16-24)	-6000	6000	V
	Pre Driver (Pin 7-15)	-2000	2000	V

According to "MIL-STD-883J Method 3015.9", under the environment of 25°C and 55% relative humidity, electrostatic discharge is applied to all IO pins of the tested chip for 3 times, with an interval of 1s each time. The test results show that the anti-static discharge level of the chip reaches Class 3A ≧4000V, <8000V.

Table 6-4 LKS32MC077EM6S8 Latch-up parameters

Item	Minimal	Max	Unit
Latch-up current (85 ℃)	-200	200	mA

According to "JEDEC STANDARD NO.78E NOVEMBER 2016", an overvoltage of 8 V is applied to all power supply IOs, and a current of 200 ma is injected on each signal IO. The test results show that the anti-latch-up level of the chip is 200 mA.

Table 6-5 LKS32MC077EM6S8 IO absolute characteristics

Parameter	Description	Min.	Max.	Unit

V_{IN}	GPIO Signal Input Voltage Range	-0.3	6.0	V
HO_x	HO_x (x=1~3) input voltage range	VCC-15	VCC	V
LO_x	LO_x(x=1~3) input voltage range	-0.3	15	V
I_{INJ_PAD}	Maximum Injection Current of A Single GPIO	-11.2	11.2	mA
I_{INJ_SUM}	Maximum Injection Current of All GPIOs	-50	50	mA

Table 6-6 LKS32MC077EM6S8 IO DC Parameters

Parameter	Description	AVDD	Conditions	Min.	Max.	Unit
V_{IH}	High input level of digital IO	5V	-	3.06		V
		3.3V		2.07		
V_{IL}	Low input level of digital IO	5V	-		0.3*AVDD	V
		3.3V			0.8	
V_{HYS}	Schmidt hysteresis range	5V	-	0.1*AVDD		V
		3.3V				
I_{IH}	Digital IO current consumption when input is high	5V	-		1	uA
		3.3V				
I_{IL}	Digital IO current consumption when input is low	5V	-	-1		uA
		3.3V				
V_{OH}	High output level of digital IO		Current = 11.2mA	AVDD-0.8		V
V_{OL}	Low output level of digital IO		Current = 11.2mA		0.5	V
R_{pup}	Pull-up resistor*			8	12	kΩ
R_{io-ana}	Connection resistance between IO and internal analog circuit			100	200	Ω
C_{IN}	Digital IO Input-capacitance	5V	-		10	pF
		3.3V				

Table 6-7 LKS32MC07x Module Current/IDD

模块	Min	Typ	Max	单位
Comparator x1		0.005		mA
OPA x1		0.450		mA
ADC		3.710		mA
DAC		0.710		mA
Temp Sensor		0.150		mA
Band-Gap		0.154		mA
4MHz RC Clock		0.105		mA
PLL		0.080		mA
CPU+flash+SRAM (96MHz)		8.667		mA

CPU+flash+SRAM (12MHz)		1.600		mA
CRC		0.070		mA
DSP		3.421		mA
UART		0.107		mA
DMA		1.340		mA
MCPWM		0.053		mA
TIMER		0.269		mA
SPI		0.500		mA
IIC		0.500		mA
CAN		2.200		mA
MCU Sleep Mode	9	12	20	uA

7 Power Management System

The power management system is composed of LDO15 module, power detection module (PVD), power-on/power-off reset module (POR).

The chip is powered by a 7.5V ~ 32V single supply to save the power supply costs outside the chip. An internal LDO5 supply the power of MCU. And all internal digital circuits and PLL modules in the MCU are powered by an internal LDO15.

The LDO15 automatically turns on after power-on, without software configuration, and the LDO output voltage can be adjusted through software.

The output voltage of LDO15 can be adjusted by setting register LDO15TRIM <2:0>. The corresponding value of the register can be seen in the analog register table. LDO15 has been calibrated before it leaves the factory. Generally, users do not need to configure these registers again. If fine-tuning of the LDO output voltage is required, please read the original configuration value first, and then add the configuration value corresponding to the fine-tuning amount to the register.

The POR module monitors the voltage of the LDO15. When the voltage of the LDO15 is lower than 1.26V, for example, at the beginning of power-on or at the time of power-off, it will provide a reset signal for the digital circuit to avoid any abnormal operation.

The PVD module detects the 5V input power supply, and generates an alarm (interrupt) signal to remind MCU if it is lower than a certain set threshold. The interrupt alert threshold can be set to a different voltage using the PVDSEL<1:0> register. You can disable the PVD module by setting PD_PDT= '1'. See the analog register table description for the corresponding values of specific registers.

8 Clock system

The clock system consists of a 32KHz RC oscillator, a 8MHz RC oscillator, an external 8MHz crystal oscillator, and a PLL.

The 32K RC clock is used in the MCU system as a slow clock for modules such as reset/wakeup source filters or used in the low power mode; The 8MHz RC clock can be used as the main clock of the MCU, and can provide a reference clock to PLL. PLL clock is up to 96MHz; The external 8MHz crystal oscillator is used as a backup clock.

Both 32k and 8M RC clocks will been through factory calibration. In the range of -40 ~ 105 ℃, the accuracy of the 32K RC clock is ±50%, and the accuracy of the 8M RC clock is ± 1%.

The frequency of the 32K RC clock can be set by the register RCLTRIM<3:0>, and the frequency of the 8M RC clock can be set by the register RCHTRIM <5:0>. For the corresponding value of specific register, please refer to the analog register table.

The chip has been calibrated before it leaves the factory. Generally, users do not need to configure these registers again. If fine-tuning of the frequency is required, please read the original configuration value first, and then calculate the new settings accordingly.

The 8M RC clock is turned on by setting RCHPD = ’0’ (ON by default, turn off when set to “1’). The RC clock needs a reference voltage and current provided by the Bandgap voltage reference module; thus, do remember to turn on the BGP module before turning on the RC clock. When the chip is powered on, the 8M RC clock and BGP module are both turned on automatically. The 32K RC clock is always on and cannot be turned off.

The PLL multiplies the 8M RC clock to provide a higher frequency clock for modules like MCU and ADC. The highest frequency of MCU and PWM module is 96MHz, and the typical working frequency of ADC module is 48MHz. It can be set to different frequency by the register ADCLKSEL <1:0>.

PLL is turned on by setting PLLPDN = ’1’ (OFF by default, turn on when set to '1'). Before turning on the PLL module, the BGP (Bandgap) module should be turned on first. After the PLL is turned on, it needs a settling time of 6us to achieve a stable frequency output. When the chip is powered on, the RCH clock and BGP module are both turned on. PLL is OFF by default and could be enabled by software.

The crystal oscillator circuit has a built-in amplifier and an oscillator capacitor. Connect a crystal between IO OSC_IN/OSC_OUT and set XTALPDN = ’1’ to start the oscillation.

9 Voltage Reference

Reference voltage and current are provided for ADC, DAC, RC clock, PLL, temperature sensor, operational amplifier, comparator and FLASH. Before using any of the above modules, the BGP voltage reference should be turned on first.

When the chip is powered on, the BGP module is turned on automatically. The voltage reference is turned on by setting BGPPD = ’0’. From OFF to ON, BGP needs about 6us to stabilize. BGP output voltage is about 1.2V, and accuracy is ± 0.8%.

10 ADC module

The chip integrated a synchronous double-sampling SAR ADC which is shut down by default when the chip is powered up. Before turning on ADC, the BGP module, 8M RC clock and PLL should be turned on first. In the default configuration, ADC clock is 48MHz, which corresponds to a conversion rate of 3Msps.

The synchronous double sampling circuit can sample the two input analog signals at the same time. After the sampling is completed, the ADC converts the two signals one by one and writes them into the corresponding data registers.

ADC takes 16 ADC clock cycles to complete one conversion, of which 13 are conversion cycles and 3 are sampling cycles. I.E. $f_{conv}=f_{adc}/16$. When the ADC clock is set to 48MHz, the conversion rate is 3Msps.

When the ADC is working at a lower frequency, the power consumption can be reduced by setting register CURRIT<1:0>.

ADC could work in different modes: One-time single channel trigger mode, continuous single channel sampling mode, One-time 1 to 20 channels scanning mode, continuous 1 to 20 channels scanning mode. It has a set of 20 independent registers for each analog channel.

The ADC trigger can be MCPWM/Timer trigger signals T0, T1, T2 and T3 happened for the preset number of times, or software trigger event.

ADC _ DC stores the DC offset of ADC. Usually, in the calibration phase, the ADC DC offset value is obtained by measuring the AVSS (internal ground) of Channel 15 (counting from 0) and stored in flash. In the system loading phase, the DC offset is written into the ADC _ DC register by software.

The ADC has two ranges set by the ADC X _ GAIN (X = 0, 1): 3.6 V and 7.2 V. At the 7.2 V range, this corresponds to a maximum input signal amplitude of ± 5 V because the chip is powered at 5 V. At the 3.6 V range, this corresponds to a maximum input signal amplitude of ± 3.6 V. When measuring the output signal of an op amp, select the specific ADC gain based on the maximum signal that the op amp can output.

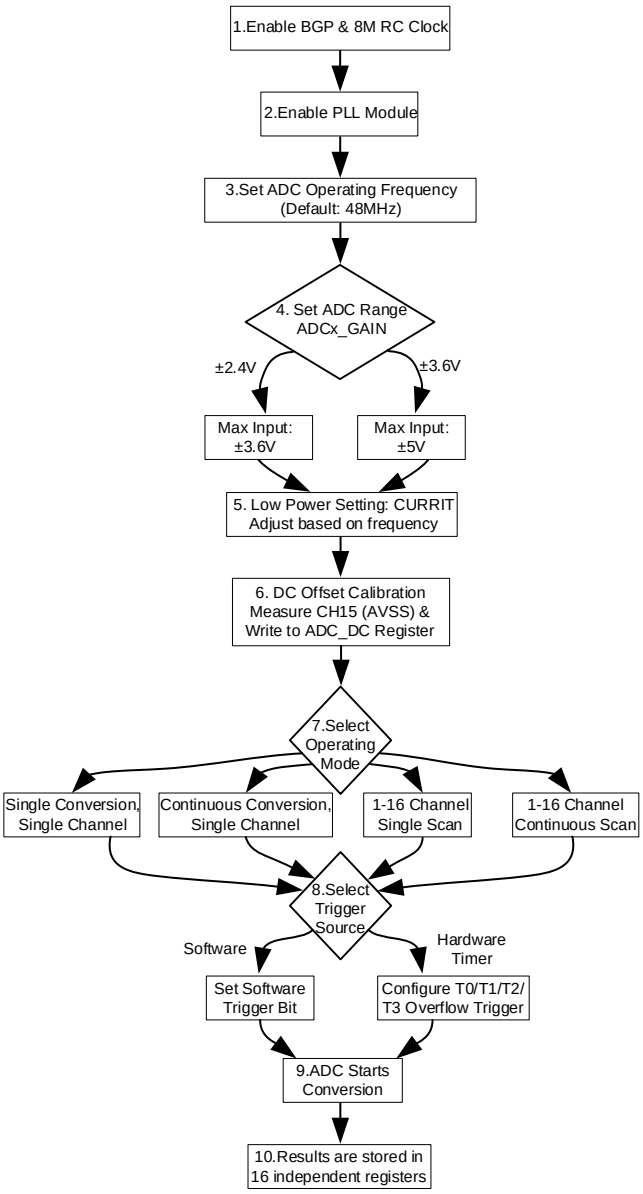


Figure 10-1ADC Configuration Flowchart

11 Operational Amplifier

4-channel of rail-to-rail OPAs are integrated, with a built-in feedback resistor R2/R1. A resistor R0 is required to be connected in series to the external pin. The resistance of feedback resistors R2:R1 can be adjusted by register RES_OPA0<1:0> to achieve different gain. For the corresponding value of specific register, please refer to the analog register table.

The close-loop gain of OPA is R2/(R1+R0), where R0 is the resistance of the external resistor.

For the application of MOS resistance direct sampling, it is recommended to connect an external resistance of >20kΩ to reduce the current flowing into the chip pin when the MOS is turned off;

For the application of small resistance sampling, it is recommended to connect an external resistor of 100Ω.

The OPA can select one of the output signals of the 4-channels amplifiers by setting OPAOUT_EN <2:0>, and send it to the P2.7 IO port through a buffer for measurement (see the corresponding relationship in the datasheet 'Pin Function Description"). Because of this buffer, the OPA is able to be output to an IO while operating normally.

When the chip is powered on, the OPA module is OFF by default. It can be turned on by setting OPAxPDN = ’1’, and turn on the BGP module before turning on the amplifier.

For built-in clamp diodes are integrated between the positive and negative OPA inputs, the motor phase line could be directly connected to the OPA input through a matching resistor, thereby simplifying the external circuit for MOSFET current sampling.

12 Comparator

Built-in 3-channel rail-to-rail comparators with programmable comparator speed, hysteresis voltage, and signal source.

The comparison delay of the comparator can be set to < 30nS/200 nS through Register CMP _ FT. The hysteresis voltage is set to 20 mV/0 mV by the CMP _ HYS.

The comparator positive input signal source can be set by register CMPx _ SELP [2:0]; the comparator negative input signal source can be set by register CMPx _ SELN [1:0] (X = 0/1/2 for comparators CMP0/CMP1/CMP2）。

When the chip is powered on, the comparator module is OFF by default. The comparator is turned on by setting CMPxPDN = ’1’, and turn on the BGP module before turning on the comparator.

13 Temperature sensor

The chip has a temperature sensor with an accuracy of ±2°C. The temperature sensor will be calibrated in factory, and the calibration value is saved in the flash info area.

When the chip is powered on, the temperature sensor module is OFF by default. Turn on the BGP module before turning on the temperature sensor.

The temperature sensor is turned on by setting TMPPDN = ’1’, and it takes about 2us to be stable after turning on. Thus, it should be turned on at least 2us ahead before the ADC measures the sensor output.

14 DAC module

The chip contains two 12-bit DACs, and the maximum range of the output signal can be set to 1.2 V/4.85 V using the DAC0 _ GAIN and DAC1 _ GAIN registers.

DAC0 can route the DAC0 output to the P0.0 pin through the configuration register DAC0OUT _ EN = 1, and DAC1 can route the DAC1 output to the P0.0 pin through the configuration register DAC1OUT _ EN = 1, which can drive a load resistor of > 5kΩ and a load capacitance of 50pF. Normally, DAC0 and DAC1 are not output at the same time to avoid signal contention.

The maximum output bit rate of DAC is 1MHz.

When the chip is powered on, the DAC module is OFF by default. DAC0 can be turned on by setting DAC0PDN = 1, and DAC1 can be turned on by setting DAC1PDN = 1. Before turning on the DAC module, you need to turn on the BGP module.

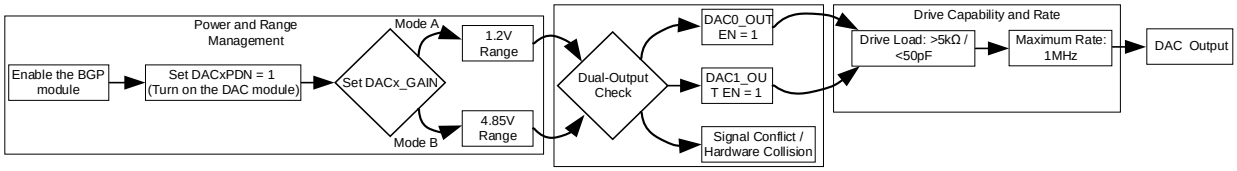


Figure 14-1DAC Configuration Flowchart

15 Processor core

- 32 bitCortex-M0 + DSP Dual Corp.Processor
- 2-wire SWD debug pin
- Maximum operating frequency 96MHz

16 Storage resources

16.1 Flash

- built-in flash including 64kB/128kB main area and 1.5kB NVR
- Endurance: 100,000 Cycles(min)
- Data retention: more than 100 years
- Single byte program: 7.5us(max), Sector erase: 5ms(max)
- Sector size 512bytes, supporting Sector erase/program and in-application program
- Flash data anti-theft by programming the last word of flash to any words other than 0xFFFFFFFF

16.2 SRAM

- built-in 12kB SRAM

17 MCPWM for motor drive

- MCPWM operating frequency is up to 96MHz
- It can generate 6 pairs of non-overlapping PWM signals (complementary mode) or 12 independent non-overlapping PWM signals (edge-aligned mode). The module consists of two chopper modules, with each group sharing one dead-time configuration.
- Support edge-aligned PWM
- Support software control IO mode
- Support IO polarity control
- Internal short circuit protection to avoid short circuit due to configuration error
- External short circuit protection, enabling fast shutdown by monitoring the external signals
- Internal ADC sampling interrupt
- Preload MCPWM register configuration and update simutaneously
- Programmable load time and period

18 Timer

- 4-channel standard timer, 2-channel 16-bit timer, 2-channel 32-bit timer.
- Support capture mode for measuring external signal/pulse width
- Support comparison mode for timed interruption of edge-aligned PWM

19 Hall sensor interface

- Built-in 1024 cycles filtering
- 3-channel Hall signal input
- 24-bit counter, with overflow and capture interrupt

20 General Purpose Peripheral

- Two UART, full-duplex operation, support 8/9 data bit, 1/2 stop bit, odd/even/no parity mode, with 1 byte tx buffer, 1 byte rx buffer, support Multi-drop Slave/Master mode, support 300 to 115200 baud rate
- One SPI, support master-slave mode
- One IIC, support master-slave mode
- Hardware watchdog, driven by 32kHz RC clock and which is independent of system high-speed clock, the minimum reset interval was 4096/32kHz≈128ms, and the maximum reset interval was 511×4096/32kHz≈64s.

21 Gate drive module

21.1 Module parameters

Table 21-1 Driver module parameter

Symbol	Parameter	Condition	Minimal	Typical	Max	Unit
Static parameters						
VCC_ON	VCC undervoltage recovery voltage		5.8	6.5	7.4	V
VCC_UVLO	VCC Undervoltage Threshold Voltage		5.4	6	6.8	V
VCC_HYS	Under-voltage voltage return difference		0.3	0.5	0.8	V
V_{HO}	HOx(x=1~3) outputs turn-on voltage (because HO drives PMOS, low level corresponds to turn-on)		VCC-11.5	VCC-10	VCC-8.5	V
V_{LO}	LOx(x=1~3) output turn-on voltage		8.5	10	11.5	V
I_{HO+}	HOx(x=1~3) output current	HOx=VCC-10V	-	300	-	mA
I_{HO-}	Input sink current of HOx(x=1~3)	HOx=VCC	-	35	-	mA
I_{LO+}	LOx(x=1~3) output current	LOx=0V	-	60	-	mA
I_{LO-}	LOx(x=1~3) Input sink current	LOx=10V	-	300	-	mA
T_{SD}	TSD temperature		-	150	-	℃
$T_{RECOVER}$	TSD recovery temperature		-	135	-	℃
I_{LDO}	LDO power supply capability			40		mA
Dynamic parameters (CL = 1 nF)						
T_{ON}	Conduction propagation delay		-	80	-	ns
T_{OFF}	Turn off transmission delay		-	30	-	
TH_R	HOx rise time		-	60	-	
TH_F	HOx fall time		-	300	-	
TL_R	LOx rise time		-	300	-	
TH_F	LOx fall time		-	60	-	
DT	Built-in dead time		-	50	-	

The input and output waveforms of the P/N MOS drive module are shown in the figure below. In the figure, HIN/LIN is the output signal of the MCPWM module inside the chip. For HIN, the output high level corresponds to the HO output low level, thus driving the high-drive PMOS to conduct. For LIN, the output high corresponds to the LO output high, which drives the low-drive NMOS on. Therefore, the polarity selection of P and N in MCPWM MCPWM _ IO01/MCPWM _ IO23 does not need to be inverted.

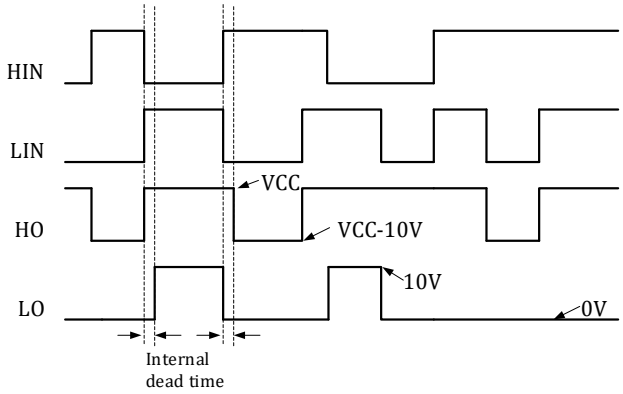


Figure 21-1 Input and output time sequence waveform of drive module

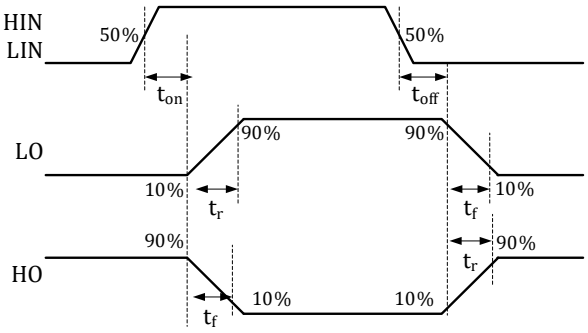


Figure 21-2 Driving module output change edge time sequence waveform

21.2 Recommended application diagram

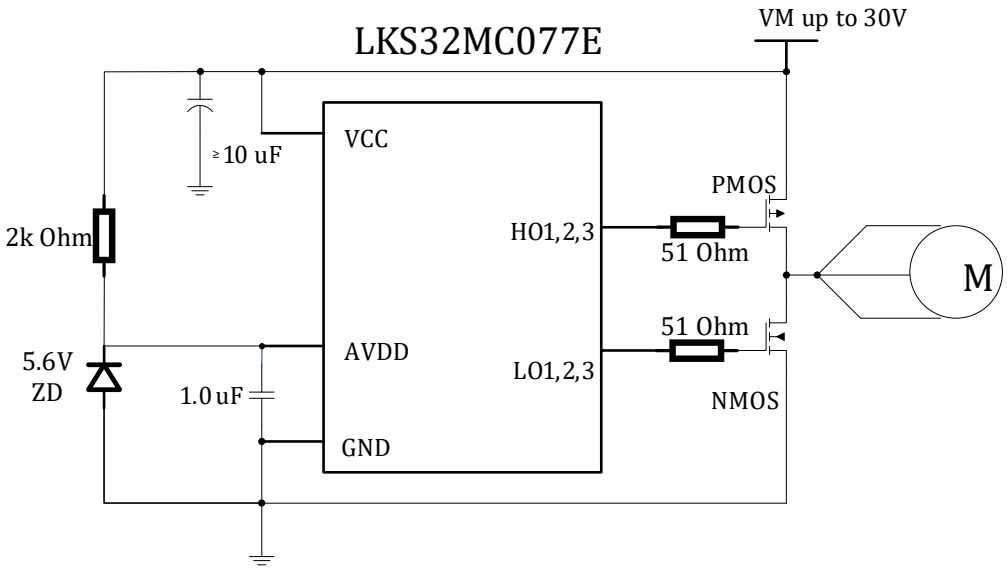


Figure 21-3 Typical Application Diagram of LKS32MC077EM6S8 Driver Module

The output pin signal LO1/HO1 of the drive module corresponds to the MCPWM function output of GPIO P1.0/P0.15 , and LO2/HO2 corresponds to the MCPWM function output of GPIO P2.12/P2.11. LO3/HO3 corresponds to MCPWM function output of GPIO P2.5/P2.4.

When the phase current is greater than 2A, it is recommended to connect a 51 ohm resistor in series between the HO1/2/3 output pin and the PMOS gate and between the LO1/2/3 output pin and the NMOS gate.

In applications where VCC is higher than 20 V and the chip does not need to sleep, it is recommended to add a 1 K to 2K ohm shunt resistor between VCC and AVDD, which is added between the input and output of the internal 5V LDO to share part of the heat dissipation function. The resistor needs to be placed some distance away from the chip.

The following formula shall be used to calculate the resistance value:

R>=(VCC-AVDD)/I

Where I is the total power consumption on the 5V power supply, including the power consumption of the MCU and the power consumption of the 5V peripheral devices (such as HALL).

With an external shunt across, place a 5.6 V regulator at the AVDD pin.

At the same time, in applications where there is a resistor between VCC and AVDD, it is important to note that the RC constant on RSTN should not be too large, and it is recommended to keep the RC constant at 1ms. That is, if the internal pull-up resistor is 100 K without adding a resistor to the outside of the chip to 5V, the capacitance on RSTN is selected to be 10 nF. If a pull-up resistor of 10 K or 20 K is added externally, the capacitance on RSTN is selected to be 100 nF.

There must be a 1uF or greater decoupling capacitor from the VCC pin to ground.

The gate drive module polarities are as follows:

Table 21-2 LKS32MC077EM6S8 Gate Drive Polarity Truth Table

{HIN, LIN}	HO	LO	
00	1	0	Upper and lower tubes are turned off
01	1	1	Lower tube conduction
10	0	0	Upper tube conduction
11	1	0	Upper and lower tubes are conducted at the same time, and hardware short circuit protection

22 Special IO multiplexing

Notes for Special IO Multiplexing of LKS07x

The SWD protocol includes two signals: SWCLK and SWDIO. SWCLK is a clock signal. To the chip, it is an input and will always be an input. SWDIO is a data signal. It switches between the input state and the output state during data transmission, and the default is the input state.

Some LKS07x SWD pins also have GPIO function. The IO multiplexed by SWCLK is P2.14 and the IO multiplexed by SWDIO is P2.15. The precautions are as follows:

- The default state of GPIO multiplexing is disabled, IO are used as SWD. After the hard reset of the chip, the initial state of IOs are SWD. Both IOs of SWD are fixed pull-up inside the chip (the internal pull-up resistor of the chip is about 10K). Please pay attention to the initial IO voltage level if application has specific requirements.
- When GPIO multiplexing is enabled, tools such as KEIL cannot directly access the chip, i.e., the Debug and erase download functions cannot access the chip since SWD are now general GPIO. If the program needs to be downloaded again, there are two solutions.
- Firstly, it is recommended to use Linko's dedicated offline downloader to erase. It is recommended to leave a certain margin before switching SWD to GPIO, such as about 100ms, to ensure that the offline downloader can erase the chip and prevent the deadlock. This margin is to ensure a successful offline downloader erasing. A greater margin means a greater probability of the successful one-time erasion.
- Secondly, the application should have a GPIO multiplexing exit mechanism. For example, some other IO invert (usually input), indicates that the SWDIO is required externally, and the software needs to be reconfigured to disable the multiplexing. At this moment, the KEIL function can access the chip via SWD again.

In SSOP24L package and QFN5*5 40L-0.75 package, SWDIO is directly bonded with P0.0 and P2.15, and the corresponding GPIO can be directly enabled. It is recommended that SWDCLK keep unchanged (constant 1 or constant 0) when multiplexing SWDIO

For LKS077E, SWDCLK is bonded with P2.6 and the corresponding GPIO can be directly enabled. If SWDIO and SWDCLK are multiplexed at the same time, considerations for SWDCLK multiplexing are as follows:

- The default state of GPIO multiplexing is disabled, IO are used as SWD. After the hard reset of the chip, the initial state of IOs are SWD. Both IOs of SWD are fixed pull-up inside the chip (the internal pull-up resistor of the chip is about 10K). Please pay attention to the initial IO voltage level if application has specific requirements.
- When GPIO multiplexing is enabled, tools such as KEIL cannot directly access the chip, i.e., the Debug and erase download functions cannot access the chip since SWD are now general GPIO. If the program needs to be downloaded again, there are two solutions.
- Firstly, it is recommended to use Linko's dedicated offline downloader to erase. It is recommended to leave a certain margin before switching SWD to GPIO, such as about 100ms, to ensure that the offline downloader can erase the chip and prevent the deadlock. This margin is to

ensure a successful offline downloader erasing. A greater margin means a greater probability of the successful one-time erasion.

- Secondly, the application should have a GPIO multiplexing exit mechanism. For example, some other IO invert (usually input), indicates that the SWDIO is required externally, and the software needs to be reconfigured to disable the multiplexing. At this moment, the KEIL function can access the chip via SWD again.

When SWDCLK and SWDIO pins are used as GPIO, they should not act at the same time. That is, when SWDCLK multiplexing is enabled and changes, SWDIO can remain at level 0 (similar to time division multiplexing).

For RSTN signal, the default is for the external reset pin of LKS07x chip.

LKS07x allow users to multiplex RSTN as other IOs, and the multiplexed IO is P0.2. The precautions are as follows:

- The default state of reset IO multiplexing is disabled, and the software needs to write 1 to SYS_RST_CFG[5] to multiplex RSTN as GPIO. I.e., the initial state of P0[2] is RSTN. RSTN is provided with a pull-up resistor inside the chip (the internal pull-up resistor of the chip is about 100K). Attention shall be paid when the application has requirements for initial electric level.
- The default state of P0[2] is used as external reset, and the program can only be executed after the RSTN is released. The application needs to ensure that the RSTN has sufficient protection, such as the peripheral circuit with a pull-up resistor. It is better to add a capacitor.
- After RST IO multiplexing is enabled, the external reset is unavailable to the chip. If a hard reset is required, the reset source can only be power-down/watchdog reset.
- The multiplexing of RSTN does not affect the use of KEIL.

Bit [5] in the SYS _ RST _ CFG register controls the switch for multiplexing RSTN and P0.2.

23 Ordering Information

Tray Package:

Package Type	Quantity per disc/tube	Quantity in box	Quantity in case
SOP16/ESOP16L	3000/ disc	6000PCS	48000PCS
SSOP24	4000/ disc	8000PCS	64000PCS
SS0P24	50/ pipe	10000PCS	4000/100000PCS
QFN 8*8	260/ disc	2600PCS	15600PCS
QFN 4*4/5*5/6*6	490/ disc	4900PCS	29400PCS
QFN 3*3	5000/ disc	5000PCS	40000PCS
LQFP48/TQFP48 0707	250/ disc	2500PCS	15000PCS
LQFP64 1010	160/ disc	1600PCS	9600PCS
LQFP100 1414	90/ disc	900PCS	5400PCS
TSSOP20/28	4000/ disc	8000PCS	64000PCS

Reel Package:

Package Type		Quantity per disc/tube	Quantity per box	Quantity boxes per case	Quantity per case
Braid -13 inches	SOP/ESOP8	4000	8000	8	64000
Braid -13 inches	SOP/ESOP16	3000	6000	8	48000
Braid -13 inches	SSOP24	4000	8000	8	64000
Braid -13 inches	TSSOP20	4000	8000	8	64000
Braid -13 inches	D/QFN3*3	5000	10000	8	80000
Braid -13 inches	D/QFN4*4	5000	10000	8	80000
Braid -13 inches	D/QFN5*5	5000	10000	8	80000
Pipe	SOP16	50	10000	10	100000
Pipe	SOP14/SSOP24	50	10000	10	100000
Pipe	TSSOP24	54	6480	6	38880

24 Version history

Table24-1Document version history

Time	Version No.	Description
2026.04.07	1.20	Revise the internal pre-drive connection diagram
2026.03.09	1.19	Revise the CMP trip voltage parameters
2026.01.26	1.18	Add the configuration description block diagram for the DAC module.
2026.01.20	1.17	Add ADC configuration flowchart
2026.01.08	1.16	Remove non-matching model types from the selection table.
2025.12.28	1.15	Revise the MCPWM module description to: Two chopper modules, with each group sharing one dead-time configuration.
2025.12.24	1.14	Retain only LQFP48 for the 07 series packaging.
2025.11.03	1.13	Revised OPA Module Common-Mode Level
2025.08.22	1.12	Update naming rules
2025.07.21	1.11	Delete the Flash section: erase/program one sector while accessing another
2025.01.02	1.1	Update the offset voltage of the CMP
2024.08.21	1.09	Add internal predrive connection diagram
2024.08.04	1.08	Order package information updates to confirm package information by package type and package form
2023.11.20	1.07	Add description of OPA offset
2023.10.22	1.06	Modify the device selection table
2023.09.25	1.05	Update welding temperature, modify non-volatile memory Sector erase description
2023.07.27	1.04	Modify/updated a new model 07x 6N in the device selection table
2023.07.04	1.03	Modify the opa output signal range, power supply range,sleep power consumption and Vcm
2023.05.07	1.02	Correct I_{HO+} and I_{HO-} current values of the gate drive module, Updated the number of times the flash can be erased repeatedly
2023.04.07	1.01	Update package description
2023.03.16	1.0	Initial version

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For earlier versions, please refer to this document.